T.M. 6793A

TECHNICAL MANUAL (CLASS B)

INSTALLATION, OPERATION
AND
MAINTENANCE INSTRUCTIONS
WITH PARTS LIST

RA6793A HF RECEIVER

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RACAL

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SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all times observe all safety regulations. Do not replace components with power on. Under certain conditions, dangerous potentials may exist when the power control is in the off position. To avoid casualities, always remove power and discharge a ground circuit before touching it.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances reach into the unit for the purpose of servicing or adjusting equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation.

Warnings and Cautions appear in the text in locations where appropriate.

WARRANTY

Seller warrants each new product manufactured and sold by Seller (except consumable items such as tubes, fuses, batteries, bulbs, and like items), that it will conform with the applicable specifications and will be free from defects in material and workmanship under normal use and service for a period of one (1) year from the date of shipment from Seller's plant when operated in accordance with Seller's operating instructions. This warranty shall extend only to the Buyer and to the United States Government, but to no others.

Warranties are valid only when and if:

(a) Seller received prompt written notice of the breach within the period of the warranty;

(b) The defective product is properly packed and returned by the Buyer (transportation and insurance prepaid); and

(c) The product is defective and has not been subjected to any misuse, neglect, improper installation, accident, unauthorized repair or alteration.

Seller's exclusive obligation under all warranties, express or implied, and Seller's exclusive liability for any personal and/or property damage (including direct, consequential and incidental) caused by the breach of any or all warranties shall be limited to repair or replacing any defective part or parts free of charge, F.O.B. Seller's plant.

Except where the product is sold to Seller's description and sole specification, Seller does not warrant Merchantability of Goods or that the product is Fit for the Purposes intended. There are no warranties that extend beyond the description on the face hereof or beyond the terms and conditions contained herein.

IN NO EVENT SHALL SUBCONTRACTOR BE LIABLE FOR ANY SPECIAL, INCIDENTAL OR CONSEQUENTIAL LOSS OR DAMAGE ARISING OUT OF ITS BREACH OF ANY PROVISION OF THIS CONTRACT.

Clearing RA6793A memory after battery replacement.

Press **CHAN** △ Light On

Change all modes and frequency to desired operating info

Press and Hold **STORE** Button

Enter "01" Release **STORE** Button (The CHANNEL will go blank)

Press and Hold **STORE** Button again

Enter "02" Release **STORE** Button (The CHANNEL will go blank)

Press **CHAN** Button again and check info stored by using the Tuning Knob to change the channel and display the stored information.

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R-2174 FORCED FILTER OPERATION

1. ENTER FORCED FILTER MODE BY PRESSING (AND HOLDING) THE **LOCK** KEYSWITCH , THEN MOMENTARILY PRESS THE **ISB U/L** KEYSWITCH. RELEASE BOTH. (THE **AUX** INDICATOR SHOULD ILLUMINATE ON THE AUXILIARY DISPLAY INDICATING FORCED FILTER MODE IS ACTIVE).

2. ENTER THE DESIRED FILTER DISPLAY VALUES. THE FILTER VALUES ARE ENTERED IN ASCENDING FILTER POSITION ORDER, 1-7. (*NOTE THAT A MAXIMUM OF* **5 SYMMETRICAL**, **1 LSB**, *AND* **1 USB** *FILTERS MAY BE ENTERED. FEWER MAY BE ENTERED, DEPENDING ON THE FILTER HARDWARE CONFIGURATION).*

BLANK FILTER SLOTS SHOULD BE ENTERED SIMPLY BY PRESSING **ENTER**, TO MOVE PAST THE SLOT.

A. SYMMETRICAL FILTERS: PRESS NUMERIC KEYPAD SWITCHES FOR FILTER VALUES, IN 100 Hz RESOLUTION STEPS. (FOR 400 Hz, PRESS "4". FOR 3.2 kHz, PRESS "3" THEN "2"). TERMINATE EACH FILTER ENTRY WITH **ENTER**.

B. **USB** FILTER: PRESS THE **USB** KEYSWITCH, TERMINATE WITH **ENTER**.

C. **LSB** FILTER: PRESS THE **LSB** KEYSWITCH, TERMINATE WITH **ENTER**.

D. NULL (BLANK) FILTER SLOT: TERMINATE WITH **ENTER**

3. TERMINATE FORCED FILTER MODE BY PRESSING THE **ISB U/L** KEYSWITCH. (NOTE THAT THE **AUX** INDICATOR EXTINGUISHES). NOTE THAT FORCED FILTER MODE WILL AUTOMATICALLY TERMINATE WITH THE 7th PRESSING OF THE **ENTER**, AS THIS WILL INDICATE TO THE RECEIVER THAT ALL FILTER SLOTS HAVE BEEN DEFINED. PRESSING **ISB U/L** EARLIER THAN THIS WILL TERMINATE FORCED FILTER MODE, LEAVING ALL UNDEFINED SLOTS IN THEIR ORIGINAL CONFIGURATION.

Gary E. Wingerd

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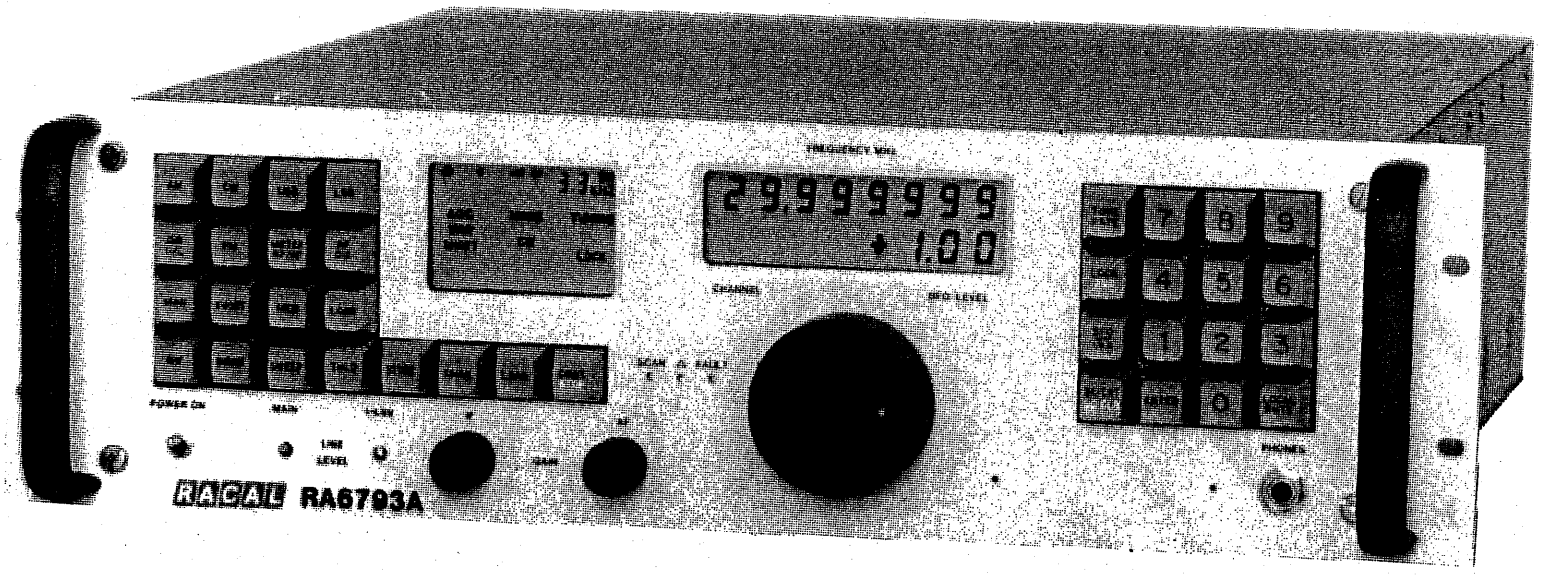


Figure 1-1. RA6793A HF Receiver

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The RA6793A HF Receiver shown in Figure 1-1 is a fully synthesized, microcomputer-based, tunable, solid state Receiver designed to provide reception capabilities for CW(A1), AM(A3), LSB/USB(A3J), FM(F3) and ISB (A3B-Optional), emissions over the frequency range of 0.5 Hz to 30 MHz. Frequency tuning is accomplished by either keyboard entry (numerical hall-effect pushbutton switches) or single knob control for continuous tuning with selectable rates, FAST (1000 Hz), SLOW (30 Hz), FINE (1 Hz) increments and BFO continuous in 10 Hz increments. Front panel indication of frequency data are presented as 8 illuminated LCD (Liquid Crystal Display) digits of tuned frequency and 3 digits and sign readout of BFO data relative to IF Center ±8.0 kHz. Other front panel displays are: RF Meter, AF Meter, Bandwidth, AGC, Mode, Tuning, Remote, Scan, Delta, and Fault Indication. Additionally, provision is made on the front panel, selectable by use of the the RF Gain Control, to manually control the AGC threshold anywhere within the range of 110 dB above the preset AGC threshold level, and the AF Gain level, selectable by used of the AF Gain control, to the Phones jack, and external loudspeaker output.

Provision is made for the selection, storage, and recall of up to 100 channels which may be preset or changed by the operator during operation. The 100 channels are divided into 10 cells, each containing 10 channels (e.g. 0-9, 10-19) which may be selectively scanned within a cell with halt on active channel exceeding a preset threshold. One to ten channels may be automatically scanned depending on the operator selected setting of each channel's scan flag. Additionally, scanning may be manually controlled by using the manual scan mode in conjunction with the main tuning knob. Channels may be preset and reviewed without disturbing normal receiver operation through use of the Delta mode. Complete RF input protection with lightening arrest is provided.

Full remote control (optional) of all receiver parameters is available by either; (1) serial asynchronous, ASCII character-oriented with strap selectable baud rate of 50 baud to 19.2 kilobaud, selectable MIL-STD-188C or EIA Standard RS-232C-C/RS-422/RS-423 compatible, 2-byte-serial, (2) byte-serial bit parallel IEEE standard 488C-1978 compatible or (3) other user specified interface format.

Built-In Test Equipment (BITE) is provided in the Receiver circuitry to find, test and report operational status to the lowest replaceable unit (LRU) with both local and remote initiation and verification.

The internal frequency tuning circuitry of the Receiver includes a single loop DIGIPHASE 1st LO Synthesizer, phase lock loop 2nd LO and BFO Synthesizers, which in combination determine tuned frequency to a resolution of 1 Hz. The synthesizer BFO tunes ±8 kHz in 10 Hz increments with a pushbutton selectable mode for immediate zero reference.

The Receiver is designed to operate with up to seven IF filters, using slots provided on the Main IF/AF circuit card assembly. Unless otherwise specified, the Receiver is factory equipped with six mechanical filters and one bypass link to provided seven selectable bandwidths. Audio output of the Receiver is either through a PHONES jack on the front panel for audio monitoring or through an AF OUT connector on the rear panel. The PHONES jack provides a nominal 10 milliwatts into 600 ohms and is adjustable through the AF GAIN

control on the front panel. The AF OUT connector provides a nominal 1 milliwatt 600 ohm balanced line output and an output of nominally 1 Watt in 8 ohms, suitable for an 8 ohm speaker.

Rear panel features include BNC connectors for providing the Receiver second IF 455 kHz output, supplying or receiving external/internal reference signals used in conjunction with a slide switch, S2. A 25-pin D-type connector provides audio, AGC and fault status outputs while an N-type connector provides RF input from an external antenna. An optional remote control interface connector, either round 26 pin (188C/232C/422/423) or elongated 24 pin (IEEE-488), is provided when specified. An IEC standard 3 prong male connector for connection of an ac line cord completes the rear panel assembly.

Input signals from the antenna are connected to a low pass filter which rejects signals above 30 Hz. The output of this filter is then coupled to a mixer stage where the RF signal is mixed with the synthesized local oscillator signal. The frequency of the local oscillator can be varied from 40.955 to 70.454999 MHz. This signal is brought through a filter and AGC controlled amplifier stages to the second mixer.

The 40.455 MHz first IF is combined with the fixed 40 MHz output from the second oscillator synthesizer to produce a 455 kHz second IF. After amplification, this second IF is routed to the plug-in 455 kHz filters which provides the main Receiver selectivity.

A second AGC-controlled amplifier follows before demodulation takes place. In the SSB/CW/AM modes, a product/synchronous detector is used. In the CW mode, the BFO synthesizer may be varied ±8 kHz (above or below the 455 kHz center frequency) through front panel controls. For FM reception, the 455 kHz second IF is input to a limiting amplifier and subsequently to a separate FM detector. All three outputs from the synthesizers are referenced to an internal 5 MHz standard frequency source, or to an external reference of 1 MHz. The demodulated signal is fed through an audio crosspoint switch to separate AF amplifiers which provide outputs for a 600 ohm line, a headphone jack, and an external loudspeaker.

For ISB operation, the optional ISB board provides the LSB signal path, while the main IF/AF board provides the USB signal path. The LSB component of the 455 kHz second IF is processed through similar circuitry with the common BFO synthesizer providing the reinserted carrier for demodulation. A separate audio amplifier provides a 600 ohm line output.

All command signals, whether from the front panel controls or from an extended or remote operating position, are processed by the microcomputer assembly. Two separate buses carry control data and address information to and from the microcomputer control assembly to the synthesizers for frequency selection, and to the appropriate switching circuits controlling the different operating modes.

1.2 MECHANICAL CHARACTERISTICS

The RA6793A Receiver mounts in a standard 19-inch (48.3 cm) equipment rack, and occupies 5.25 inches (13.33 cm) of vertical space, 19 inches (48.3 cm) wide, 18.5 inches (47 cm) deep and weighs 32 pounds (14.5 kg).

A rigid, die-cast full width chassis is used as the main frame of the receiver. Mounted within compartments on the underside of this chassis are the mixer boards and the frequency generation system. The input low pass filter, main IF/AF, optional ISB IF/AF and power supply modules are located on the top surface of the die-cast chassis while the control and digital I/O modules are attached on the Receiver main frame. All modules are accessible

for maintenance and can be removed or replaced using simple hand tools without the use of a soldering iron.

Manual controls and indicators for operation and monitoring of the Receiver are contained on the front panel while input/output jacks and connectors are provided on the rear panel. A PHONES jack, for audio connection to optional headphones, is contained on the front panel for convenient access. A primary power fuse is accessible from the rear panel.

1.3 EQUIPMENT SUPPLIED

The equipment supplied consists of the following:

1. RA6793A HF Receiver configured with assemblies:
   - A1 RF Low Pass Filter Module
   - A2 1st Mixer
   - A3 2nd Mixer
   - A4 Main IF/AF Converter
   - A6A2 Microprocessor
   - A7 1st LO Synthesizer
   - A8 2nd LO/BFO Synthesizer
   - A9 Front Panel
   - A10 Power Supply Module
2. W18, Primary Power Input Cable
3. Connector, Mating for J3
4. Six Mechanical Filters.
   Unless otherwise specified the filters shall conform to Racal part numbers 07883-1 thru 07883-6. Refer to Paragraph 1.5, Item #2 below for details.

1.4 EQUIPMENT REQUIRED BUT NOT SUPPLIED

All equipment required for normal installation and operation of the Receiver is supplied and listed in Paragraph 1.3. Maintenance equipment required for the receiver, but not supplied, is listed in Table 1-1.

Table 1-1. List of Equipment Required But Not Supplied

EQUIPMENT	MANUFACTURER
Oscilloscope, Dual Trace, Portable AN/USB-425(v)1	Tektronix 465M
RF Millivoltmeter	Boonton 92B
Spectrum Analyzer	Hewlett Packard Main Frame HP141T IF Tuning Sec. HP8552A RF Tuning Sec. HP8553B
HI-Impedance Probe, Spectrum Analyzer	Hewlett Packard HP1121A
Distortion Analyzer	Hewlett Packard 334AW/OPTH05
SG-1093/ AM/FM Signal Generator	Hewlett Packard 8640B-001

Table 1-1. List of Equipment Required But Not Supplied (Cont.)

EQUIPMENT	MANUFACTURER
Cable Coupler	Sealectro 51-075-6801
Junction Box	Racal A08047
X10 Oscilloscope Probe	Tektronix P6105X10
Frequency Counter	Hewlett Packard 5354A
RF Probe	Boonton 91-12F
50 ohm Adapter	Boonton 91-8B
Headphone Set	Racal/Amplivox V31B

a. Speaker panel
b. Mono headphones

1.5 OPTIONAL EQUIPMENT

The following features are available as standard options to the basic hardware for the RA6793A Receiver. These standard options include: remote control operations using either RS-232C or IEEE-488C remote control interface (A6A1); independent sideband (ISB) demodulation; RF signal input pre-amplification and 30 MHz low pass filtering; a low frequency (LF) tuning range extension to 20 kHz or 10 kHz; a 5 MHz high stability reference. A 100 kHz or 15 kHz If output: and, a 1 MHz wide bandwidth 1st IF output.

1. Independent Sideband Module (ISB, A5);
2. Selectable IF Bandwidth Mechanical Filters:

BANDWIDTH	DESCRIPTION	SHAPE FACTOR 3 dB : 60 dB	RACAL NUMBER
1.0 kHz	Symmetrical BPF	1:4.5	07883-2*
0.3 kHz	Symmetrical BPF	1:6.7	07883-1*
3.0 kHz	Symmetrical BPF	1:2.7	07883-3*
4.0 kHz	Symmetrical BPF	1:2.5	3600001
5.0 kHz	Symmetrical BPF	1:2.5	3600002
6.0 kHz	Symmetrical BPF	1:2.3	07883-4*
450 Hz to 3000 Hz	ISB/USB BPF	1:1.92	07883-5*
450 Hz to 2700 Hz	ISB/LSB BPF	1:1.92	07883-6*
350 Hz to 2700 Hz	USB BPF	1:1.66	08669**
300 Hz to 2200 Hz	USB BPF	1:1.97	08771**

*Standard
**Optional

Note that input and output matching capacitors are required with mechanical filters only. These are contained on assembly A4.

3. Selectable IF Bandwidth Crystal Filters:

The Receiver may be operated with one to seven different crystal bandwidth filters. There are currently a total of 23 different filters available; however, depending on Receiver configuration, some filters are mandatory. (Refer to the Installation Section of this manual for definition of IF Bandwidth Filter Installation.)

BANDWIDTH	DESCRIPTION	SHAPE FACTOR 3 dB:60 dB	DIFFERENTIAL DELAY uS	RACAL NUMBER
1.0 kHz	Symmetrical BPF	1:6	25	3600003
3.0 kHz	Symmetrical BPF	1:6	13	3600004
6.0 kHz	Symmetrical BPF	1:6	10	3600005
1.0 kHz	Symmetrical BPF	1:2.5	1080	3600006
3.0 kHz	Symmetrical BPF	1:2.5	360	3600007
6.0 kHz	Symmetrical BPF	1:2.5	180	3600008
0.125 kHz	Symmetrical BPF	1:5.33	-	08699
0.4 kHz	Symmetrical BPF	1:6.2	-	08406
1.2 kHz	Symmetrical BPF	1:6	-	08407
6.8 kHz	Symmetrical BPF	1:3.3	over 80%	08408
350 Hz to 3050 Hz	ISB/LSB BPF	1:1.6	800	08409
350 Hz to 3050 Hz	ISB/USB	1:1.6	800	08410
0.4 kHz	Symmetrical BPF	1:2.5	2000	08411
1.2 kHz	Symmetrical BPF	1:2	1000	08412
3.24 kHz	Symmetrical BPF	1:1.33	1000	08413
6.8 kHz	Symmetrical BPF	1:2	1000	08414
16.0 kHz	Symmetrical BPF	1:2	40	08415
0.5 kHz	Symmetrical BPF	1:6	80	08416
1.0 kHz	Symmetrical BPF	1:6	40	08417
2.0 kHz	Symmetrical BPF	1:6	20	08418
3.0 kHz	Symmetrical BPF	1:6	20	08419
6.0 kHz	Symmetrical BPF	1:6	20	08420
0.075 kHz	Symmetrical BPF	1:6.67	-	08589

4. Remote Control Options (A6A1):

   a. RS-232/RS-422/RS-423 Serial Asynchronous Remote Interface Module
   b. IEEE-488-1978 Compatible;

5. Improved internal frequency standard ± 3 parts 10^{-9};
6. RF Amplifier for greater receiver sensitivity;
7. Low Frequency Extension to 10 kHz;
8. Broadband IF output.

1.6 OPTIONAL EQUIPMENT HARDWARE

The equipment hardware associated with each of the standard options for the RA6793A Receiver consists of the following:

- RF Pre-Amplifier Module Assembly (A1)
- 5 MHz High Stability Reference Module Assembly (A11)
- IF Converter Circuit Card Assembly (A14)

- RS-232C Remote Control Interface Circuit Card Assembly (A6A1)
- IEEE-488C Remote Control Interface Circuit Card Assembly (A6A1)
- (1st IF OUTPUT) 2.14 MHz Wideband Converter Circuit Card Assembly (A13)
- Independent Sideband (ISB) Module Assembly (A5)
- Rack Slide Kit
- Low Frequency (LF) Extension to 20 kHz Assembly
- Low Frequency (LF) Extension to 10 kHz Assembly.

1.6.1 RF Pre-Amplifier Module Assembly (A1)

This module assembly, to be located inside the rear panel of the modified receiver main chassis and mounted in lieu of the RF low pass filter module assembly (A1), provides the following features:

- 30 MHz low pass filter
- Prevents spurious 1st LO radiation
- Improves gain and noise figure
- Provides isolation between modified receiver and RF signal input antenna for modified receiver protection
- Easily strapped in or out of RF signal path
- External muting and RF Protection circuitry.

1.6.2 5 MHz Stability Reference Module Assembly (A11)

This module assembly, to be mounted between the power supply module assembly (A10) and the ISB module assembly (A5), provides the following features:

- Greater frequency stability during independent sideband (ISB) signal detection
- Increases frequency stability from ± 5 parts 10^8 ($\pm .7$ Hz) to ± 2 parts 10^9 ($\pm .035$ Hz).

1.6.3 IF Converter Circuit Card Assembly (15 kHz through 100 kHz) (A14)

This circuit card assembly, to be mounted above the ISB module assembly (A5), provides the following features:

- Contains a 15 kHz to 100 kHz IF signal conversion stage in 5 kHz steps
- Upright and inverted frequency spectrum controlled by DIP switches
- Allows frequency deviation from 455 kHz second stage (main) IF output.

1.6.4 RS-232C Remote Control Interface Circuit Card Assembly (A6A1)

The RS-232C remote control interface circuit card assembly, to be mounted on the right side panel adjacent to the microcomputer circuit card assembly (A6A2), provides for modified receiver communication with a remote controller/computer, via a suitable data/control interface bus. The data character code used for implementing remote control operation, is the standard ASCII format; consisting of a start bit, seven data bits, a parity or stop bit (if a parity bit is not used), and a stop bit. Refer to Figure 3-2 for data character format, and to Table 3-1 for the ASCII character code identification chart. In addition, refer to Figure 7-6 for circuit details and Table 6-8 for replaceable component listing.

The input/output electrical interface provides separate lines for command input and monitor output data, allowing up to twelve receivers to be integrated on a common parallel input/output interface bus. In addition, a mating connector is supplied for interconnection

to the remote control interface connector A6A1W1J1. Refer to Section II, Paragraph 2.3.4.6 for detailed information on remote control interface connector wiring and refer to Appendix A for additional information describing the input/output control messages and command monitor data format for implementing remote control using a remote controller/computer.

1.6.5 IEEE-488C Remote Control Interface Circuit Card Assembly (A6A1)

The IEEE-488C remote control interface circuit card assembly provides an electrical interface for communication with a remote controller/computer via a suitable data/control interface bus. In addition, interconnections between the RA6793A receiver and the remote controller/computer are made through a multi-pin remote control interface connector A6A1J2, located on the receiver rear panel. Refer to Appendix B for interface requirements and receiver addressing with detailed information on command word formatting.

Communication between the remote controller/computer and the modified receiver is achieved through messages composed of data words (bytes) in serial strings. Each string of data is prefixed with a primary address for talker and/or listener operation (MTA or MLA byte). To initialize communication, the remote controller/computer sends a binary address code to the modified receiver. This binary coded decimal (BCD) address must be preset on a miniature five switch address switch assembly (S1), located on the IEEE-488C remote control interface circuit card assembly, before installation of the equipment.

The IEEE-488C remote control interface circuit comprises three primary functional circuit elements which include; a bus driver/receiver circuit, general-purpose interface adpator (GPIA) circuit, and microprocessor interrupt circuit. This circuit implements control operations utilizing eight data lines DI01-DI08, three handshake lines, DAV, NDAC and NRFD, and five bus-management lines EOI, IFC, SRQ, ATN and REN.

1.6.6 (1st IF Output) 21.4 MHz Wideband Converter Circuit Card Assembly (A13)

This circuit card assembly, to be located in place of the ISB module assembly (A5), provides the following features.

- 1 or 5 MHz wide bandwidth centered at 21.4 MHz 1st IF output

1.6.7 Rack Slide Kit

The rack slide kit consists of two rack slide mounts, Part Number 81799, and associated metal spacers and mounting hardware which are attached to the sides of the modified receiver via standard EIA hole spacings. The rack slide kit provides the following features.

- Accommodates equipment mounting in a standard 19" equipment rack
- Facilitates removal from an equipment rack

1.6.8 Low Frequency (LF) Extension to 20 kHz Assembly

The LF extension to 10 kHz assembly utilizes three different circuit card assembies and new software which provide for allowing the modified receiver to be tuned to 10 kHz. This increases the frequency range from 500 kHz - 30 MHz to 10 kHz - 30 MHz. The circuit card assemblies replaced are as follows: 1st mixer (A2), 2nd mixer (A3), and 1st LO

synthesizer (A7). In addition, the ROMSET of the standard receiver is replaced with a ROMSET which incorporates the 10 kHz frequency extension, and some BITE modifications.

1.6.9 Low Frequency (LF) Extension to 10 kHz Assembly

The LF extension to 10 kHz assembly is identical in description as the 20 kHz assembly, however, the modified receiver is now allowed to be tuned to 10 kHz. When incorporating the 10 kHz assembly the modified receiver frequency range is 10 kHz to 30 MHz.

1.7 REFERENCE DATA

Table 1-2 identifies the technical specifications for the RA6793A HF Receiver. The Receiver provides reception capabilities for CW(A1), AM(A3), LSB/USB(A3J), FM(F3) and optionally ISB(A3B) operation. Figure 1-2 depicts the International Reception Mode Codes.

Complete Designation Example:

2	A	2	H
Bandwidth in kHz	Type of Transmission	Purpose	Supplementary Characteristics
	A = AM F = FM P = PCM	0 = No modulation 1 = Telegraphs (on-off) 2 = Telegraphy (modulation) 3 = Telephone 4 = Facsimile 5 = Television 6 = Duplex Telegraphy 7 = Multichannel Telegraphy 9 = None of the above	A = Single Sideband, reduced carrier B = Two independent sidebands C = Single sideband vestigial D = AM pulse E = Pulse width modulation H = Single sideband, full carrier J = Single sideband, suppressed carrier (None) (None) = Double sidedband, full carrier

Abbreviations:

AM = Amplitude Modulation
CW = Continuous Wave
FM = Frequency Modulation (or Phase)
FSK = Frequency Shift Keying
ISB = Independent Sideband
LSB = Lower Sideband
MCW = Modulated Continuous Wave
PCM = Pulse Coded Modulation
SSB = Single Sideband
USB = Upper Sideband
DSB = Dobule Sideband

Figure 1-2. International Reception Mode Codes

Table 1-2. RA6793A HF Receiver Specifications

Frequency Range	0.5 kHz to 29.999999 MHz
Frequency Resolution	1 Hz increment
Frequency Tuning	By pushbuttons, channel scanning or continuous tuning with selectable rates, FAST (1000 Hz), SLOW (30 Hz), and FINE (1 Hz) increments; BFO continuous in 10 Hz increments.
Frequency Indication	8 digit illuminated electronic readout of tuned frequency to 1 Hz; 3 digit and sign readout of BFO relative to IF center ±8.00 kHz.
Frequency Stability	±5 parts in the 10^8 per 10°C temperature increment over the range of 0°C to 50°C using internal 5 MHz reference oscillator. Provision for an external 1, 5 or 10 MHz reference input/output. 0 dBm nominal into 50 ohms.
Detection Modes	CW/A1 Continuous Wave; CW/A2 Modulated Continuous Wave; USB/LSB (upper/lower sideband) A3A, A3H, A3J, A2A, A2H, A2J; AM/A3 Amplitude Modulation; A4 (Facsimile) ISB/A3B Independent Sideband (optional); FM/F3 Telephony.
Gain Control Modes: AGC	Control Range: An increase of 110 dB above AGC threshold will result in a change of output of less than 3 dB. Threshold Range (preset): -113 dBm to -100 dBm Time Constants: Attack: 20 msecs max. Decay: Short < 30 msecs max. Medium 200 ±100 msecs Long 3.75 secs ±1.25 secs
Manual/Automatic Gain Control	Provision is made on the front panel to select, and by use of the RF Gain Control, to manually control the AGC threshold anywhere within the range of 110 dB above the preset AGC threshold level.
Input Impedance	50 ohms nominal, 2:1 VSWR Type N Connector
Synthesizer BFO	±8 kHz in 10 Hz steps
Noise Figure	< 15 dB
Sensitivity (500 kHz to 30 MHz) 1. SSB 2. AM	 -113 dBm(0.5 uV) for 10 dB (S+N)/N Ratio. -99 dBm (2.5 uV) for 10 dB (S+N)/N Ratio in a 6 kHz bandwidth.

Table 1-2. RA6793A HF Receiver Specifications

Overall Selectivity (Standard Mechanical Filter Complement)	A wide variety of mechanical and crystal filters is available for optional requirements such as general purpose, low ripple, low shape factor, controlled delay, or linear phase. The standard filter complement is provided by six mechanical filters that are supplied with the receiver. This includes two sideband filters and four symmetrical filters. The seventh filter slot is linked in order to provide a fifth symmetrical bandwidth defined by the selectivity of the 20 kHz roofing filters. The -3 dB and -60 dB bandwidths are defined as follows: USB -3 dB 450 Hz to 3000 Hz -60 dB -600 Hz to 4300 Hz LSB -3 dB -450 Hz to -3000 Hz -60 dB 600 Hz to -4300 Hz The remaining five bandwidths are symmetrical: BW1 -3 dB 300 Hz -60 dB 2 kHz BW2 -3 dB 1 kHz -60 dB 4.5 kHz BW3 -3 dB 3.2 kHz -60 dB 8 kHz BW4 -3 dB 6 kHz -60 dB 15 kHz BW5 -3 dB 20 kHz -60 dB 80 kHz
Intermodulation (Out of Band)*	For signals 100 kHz or more from receiver tuned frequency the third order intercept point is greater than +30 dBm. Second order intercept point is greater than +60 dBm. *Below 1.5 MHz these limits may be exceeded.
Intermodulation (In Band)	Better than -50 dB for two -10 dBm input signals within the IF passband when measured at the IF or line AF output.
Cross Modulation	The level of a 30% modulated signal, 50 kHz off-tune necessary to cross modulated an on-tune carrier to a depth of 3% shall be greater than +21 dBm (2.5 volts).
Blocking	1. On Tune: Less than 10% distortion for +13 dBm (1 volt) 30% Modulated AM input signals. 2. Off Tune: 1 dB on a 30% modulated on-tune signal when in the presence of a +23 dBm (3 volt) unmodulated carrier 50 kHz off-tune.

Table 1-2. RA6793A HF Receiver Specifications

Reciprocal Mixing	The apparent noise appearing at the receiver input when in a 3 kHz bandwidth, caused by a 0 dBm signal 100 kHz off tune is less than -100 dBm.
Image and Spurious Rejection	Greater than 80 dB, for signals is least ±50 kHz from tuned frequency.
Internal Spurious Responses	<-123 dBm.
Outputs	1. IF: Frequency 455 kHz, Impedance 50 ohms, Level -10 dBm nom. Connector BNC. 2. Following outputs available at rear panel audio connector (25 pin Type D). AF: 100 Hz to 16 kHz for 3 dB flatness response. a. 1 W nominal into 8 ohm load. Distortion <3% at 500 mW. b. Monitor: Metered AF line output. 1 mW, 600 ohms balanced <2% distortion. All receiver modes selectable at front panel. c. Line 1. AF line output. 1 mW, 600 ohms balanced<2% distortion. Operable only with ISB option. All modes selectable at front panel except LSB. d. Line 2. AF line output. 1 mW, 600 ohms balanced<2% distortion. Operable only with ISB option, LSB mode. AGC: Diversity Connection with ground which provides dc voltage 10 volts to 4 volts to signal levels between threshold and +110 dB. Similar connection for ISB channel when fitted. Fault: Indication of fault condition is available at the rear panel. 3. Phone: 30 mW max. into 600 ohm load. Distortion<3% at 10 mW. Connector: Front Panel Phone Jack 4. REFERENCE OUT: Selectable TCXO Reference frequency of either 1, 5, or 10 MHz (selected by links on A8 assembly). Connector: Rear panel BNC
Environmental	1. Operating Temperature: 0°C to 50°C 2. Operating Humidity: 10% to 85% non-condensing. 3. Altitude: Operation to 15,000 ft. 4. Bench Handling: MIL-STD-810C, Method 516.2, Procedure V. 5. Vibration: MIL-STD-810C, Method 514.2, Procedure X.

Table 1-2. RA6793A HF Receiver Specifications

Storage Conditions	1. Temperature Range: -40°C to +70°C 2. Relative Humidity: 10% to 95% non-condensing. 3. Altitude: Up to 40,000 feet. 4. Fungi: Fungi identified in MIL-STD-810C, Method 508.1, Procedure I.
Power Consumption	Less than 40 VA (nominal)
Power Requirements	115/230 Vac ±10%, 48 Hz to 420 Hz, single phase.
Dimensions	Suitable for 19 inch (48.3 cm) rack or desk top console mounting: Height: 5.25 in. (13.33 cm) Width: 19 in (48.3 cm) Depth: 18.5 in. (47 cm)
Weight (approximate)	32 lbs (14.5 kg)

SECTION II

INSTALLATION

2.1 UNPACKING AND INSPECTION

It is recommended that the shipping carton containing the RA6793A HF Receiver be examined for damage before the Receiver is unpacked. If damage to the carton is observable, try to have the carrier's agent present when the equipment is unpacked. If this is not possible, retain the shipping cartons and padding material for the carrier's inspection if damage to the equipment is evident after unpacking.

No special unloading equipment is required, except to handle the carton with normal care given to any shipping carton containing electronic equipment. Figure 2-1 and 2-2 shows the critical dimensions and packaging details associated with the RA6793A HF Receiver. To unpack the Receiver, the following procedure should be observed:

1. Carefully open the top of the shipping carton and fold back the flaps.
2. Lift out the top foam cushion.
3. Carefully lift out the wrapped receiver.
4. Remove the strapping from the receiver.
5. Carefully lift out the receiver.
6. Place the receiver on a convenient work bench.
7. Replace all packaging material back in the shipping carton. Save all material in the event that the Receiver must be reshipped.

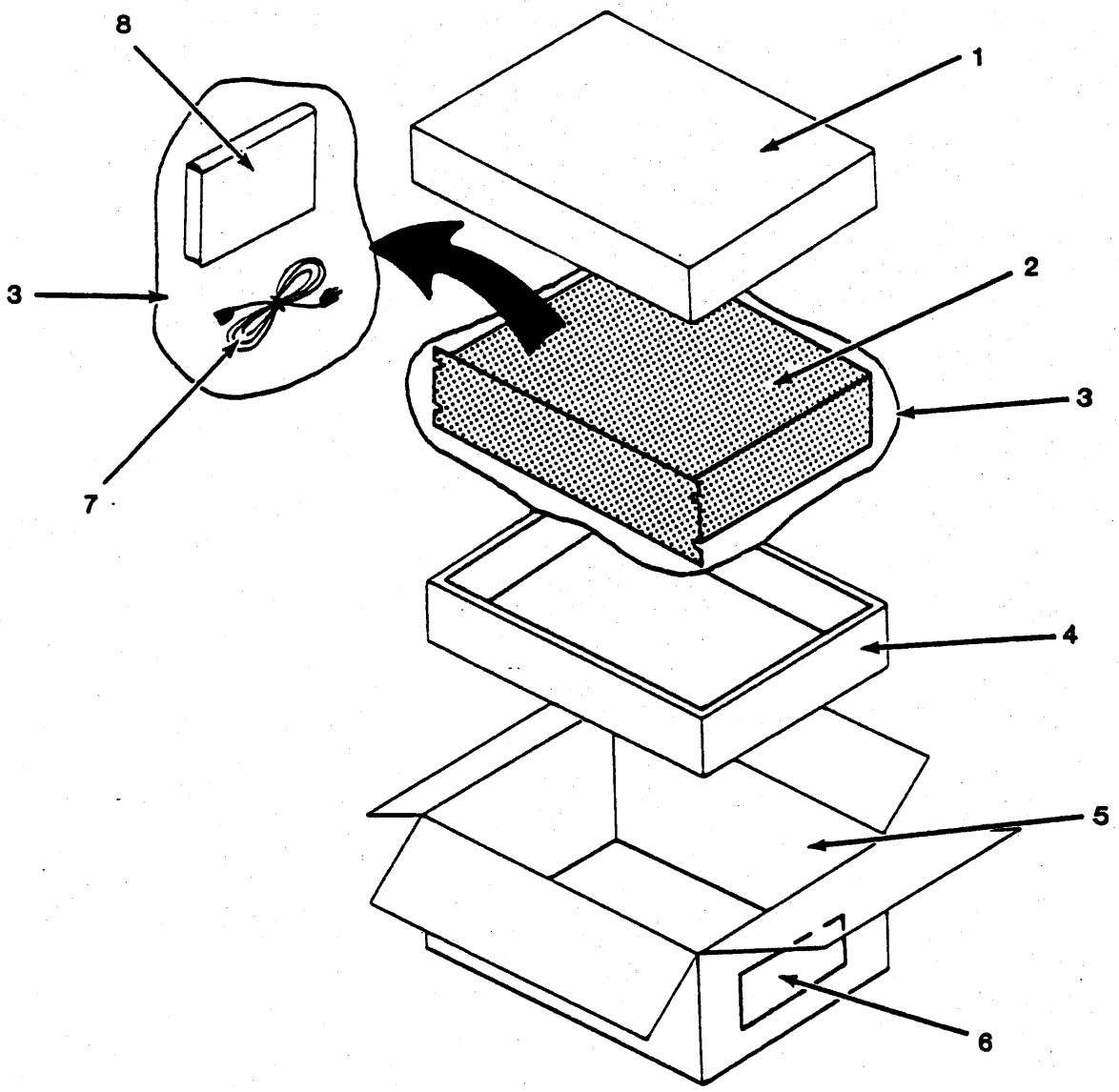
See that the equipment is complete as listed on the packing slip. Contact you RACAL representative or RACAL Communications, Inc., Rockville, Maryland with details of any shortage.

The unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. It is, therefore, ready for use upon receipt. After uncrating and checking contents against the packing slip, visually inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the dust covers and inspect the internal components for apparent damage. Then check the internal cables for loose connections, and plug-in items which may have been loosened from their receptacles.

2.2 PREPARATION FOR RESHIPMENT AND STORAGE

If the RA6793A must be prepared for reshipment, the packaging methods should follow the pattern established in the original shipment. If retained, the original materials can be used to a large extent or will at a minimum provide guidance for the repackaging effort. The Receiver must be disconnected and removed from its mounting rack before being prepared for reshipment. The following procedures describe the recommended sequence.

1. Disconnect primary power cable W18 from its primary power source. Disconnect the other end of the cable from A10J1 on the rear panel of the Receiver.
2. Disconnect the antenna cable from J1-RF IN on the rear panel.
3. Disconnect the ground strap from the GROUND lug located on the rear panel.
4. Remove any other equipment or cables connected to connectors or jacks on the rear panel.



1. Top Cover
2. RA7693A HF Radio Receiver
3. Plastic Bag
4. Bottom Piece
5. Shipping Container
6. Packing Slip
7. Power Cord
8. Technical Manual

Figure 2-2. Packaging Details, RA6793A HF Receiver

5. Remove headphones, if they are inserted from the PHONES jack located on the front panel.

6. Remove the four mounting screws from the front panel securing the Receiver to the mounting rack.

WARNING

The Receiver weighs approximately 32 pounds. Be careful as the unit is removed from the rack. Have a firm grip on the handles as the weight leaves the rack so that it does not drop, causing injury to legs or feet.

7. Grasp the Receiver by handles on the front panel and slide the unit out of the rack. Place the unit on a bench.

The unit must be housed (stored) from inclement weather in any structure that will sustain a temperature between -40° and +70°C and a relative humidity of 10 to 95 percent. The unit has an indefinite shelf life stored under the above conditions except for the nickel cadmium battery contained on circuit module board A6A2.

2.3 INSTALLATION

The Receiver is designed to be mounted in a standard 19-inch rack. The sides of the Receiver have been drilled and tapped to accept the following suggested slides (Johnathan 110-Q). The use of slides however, is optional and is dependent on the individual site requirements. If slides are installed, it is recommended that cable retractors be used to simplify extending the Receiver out of the rack. If the unit is rack mounted without the slides, access to the rear panel must be provided for connection of cables and test equipment. The power dissipation of the Receiver is approximately 40 watts with about half of the power as heat. In most installations, special cooling will not be required. The top and bottom covers on the Receiver, as well as the heat sinks on the rear panel, must be unobstructed to permit proper air circulation. Critical dimensions of the RA6793A HF Receiver are shown in Figure 2-1.

2.3.1 Rear Panel Jacks, Switches and Connectors

Access to the rear panel should be allowed so that input and output connections can be conveniently made or changed if desired. All connections except for the headphones are made from the rear of the receiver. A brief description of each rear panel switch and connector indicating function and input/output parameters is presented. Figure 2-3 presents the rear panel view of the Receiver showing the locations of the jacks, switches and connectors.

2.3.1.1 A10J1 Power Input Connector and Voltage Selector/Fuse Block Assembly

This multi-function assembly contains a three prong male power receptacle for attaching the power input cable, W18; hinged plastic FUSE PULL lever; line voltage select PC wafer and line fuse, F1. The power input cable is type BELDEN 17250.

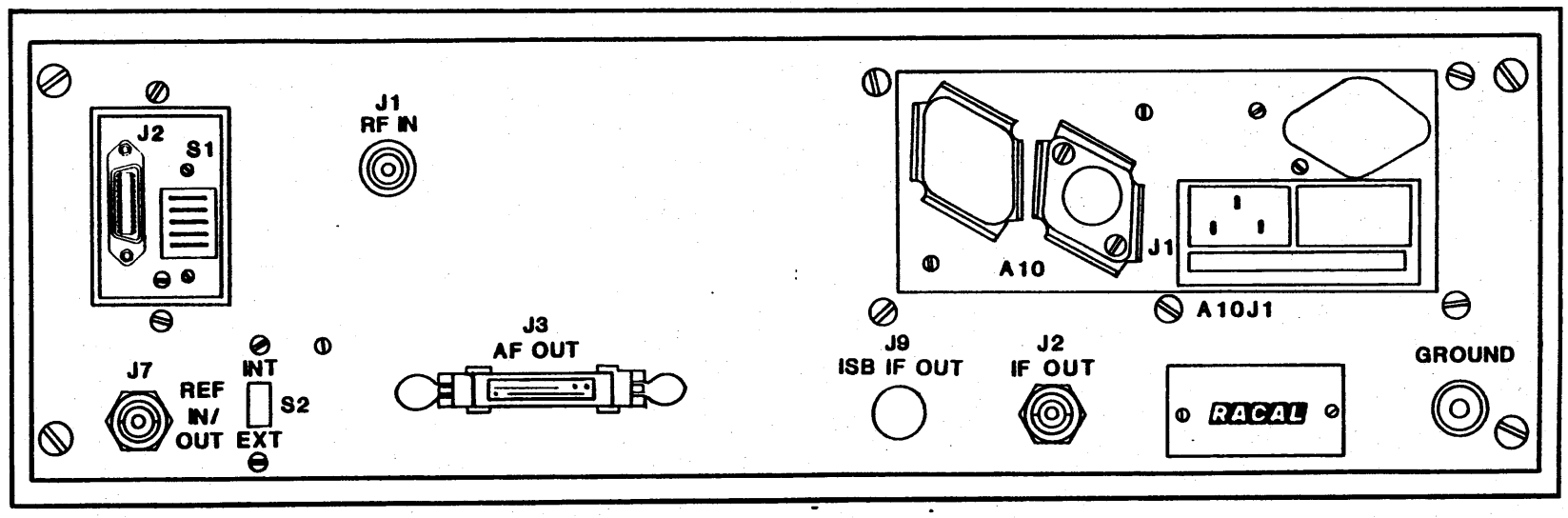


Figure 2-3. Rear Panel Jack, Switches and Connectors

CAUTION

Verify that the PC wafer in A10J1 on rear panel matches the available line voltage.

2.3.1.2 RF IN J1 Connector

The RF input from the antenna to the Receiver is made through the rear panel connector, J1. This connector is a standard N-type female connector and will mate with any standard N-type male connector. The input impedance at the connector is 50 ohms, unblanced, with a VSWR of 2:1 over the operating frequency range of the Receiver.

2.3.1.3 IF OUT J2 Connector

The second IF output signal at 455 kHz is supplied by this female BNC-type connector which will mate with any standard male BNC-type connector. The output signal level at the connector is -10 dBm $\pm$2 dB for all CW input signals within the range of -113 dBm to +13 dBm with AGC selected. The impedance of the IF output is 50 ohms with a maximum VSWR of 1.5:1.

2.3.1.4 AF OUT J3 Connector

This rear panel output connector is a female 25-pin D-type connector providing audio, AGC and fault status outputs. The audio output frequency response at this connector is within 3 dB between frequencies of 100 Hz and 16 kHz. The following audio outputs are available:

1. Loudspeaker Output. An unbalanced output capable of<5% distortion for 1 W nominal into an 8 ohm load.
2. Monitor Line Output. A metered line output for receivers which do not contain the ISB option. Switchable between USB and LSB components, from the front panel when ISB installed. Provides a 1 mW output at 600 ohms. The amplitude level is adjustable from the front panel.
3. Line 1. Line output for the USB component when the ISB is installed. Output is 1 mW at 600 ohms balanced. Front panel adjustable.
4. Line 2. Line output for the LSB component in the ISB operating mode. Output is 1 mW at 600 ohms balanced.
5. PHONES. This unbalanced output is capable of 10 mW at 600 ohms and is available through a front panel jack.

If the Receiver is not equipped for ISB operation, the Line 1 and Line 2 outputs are not used. The Monitor Line output, Loudspeaker output, and the front panel PHONES jack provide the audio output for the Receiver for all operating modes. When the Receiver is equipped for and is operating in the ISB mode, the Line 1 output will contain the USB audio and the Line 2 output will contain the LSB audio. The Monitor Line and Loudspeaker outputs, along with the front panel PHONES jack will provide either USB or LSB audio as controlled by the front panel ISB U/L pushbutton. With the Receiver equipped for ISB operation but not operating in the ISB mode, the Line 1, Line 2, Monitor Line, and Loudspeaker outputs, along with the front panel PHONES jack, provide their respective audios.

Other outputs available at this connector are the AGC and Fault indicator outputs.

The Main IF and ISB-LSB AGC Monitor/Input terminals may be used to control the AGC for diversity combining or to monitor the AGC voltage. For diversity combining, the Main IF AGC signal (on pin 32 of J3) of one receiver may be connected to pin 21 of the second receiver. If the Receiver is equipped for ISB operation, pin 22 of one receiver may be connected to pin 22 of the second receiver. The AGC circuits in both receivers will automatically respond to the largest signal. The Fault Indicator output will be high (logic 1, +2 Volts to +5 Volts) when a fault is not present in the Receiver. This output will go low (logic 0, 0 Volts to +0.8 Volts) when one of the synthesizer circuits has failed.

2.3.1.5 REF IN/OUT J7 Connector

This rear panel connector is used in conjunction with Slide Switch, S2. Depending on switch position, the Receiver will either accept an external 1 MHz reference input or supply a 1 MHz reference output through J7. The circuitry has an input impedance of 50 ohms and will operate with peak-to-peak signal levels of 1.0 V, ±0.5 V. The J7 connector will mate with any standard male BNC-type connector. Additionally, provision for changing the reference frequency to either 5 MHz or 10 MHz is available by making link changes (Refer to Paragraph 2.3.4 and 2.3.4.5, Receiver System Connections) on the A8 assembly.

2.3.1.6 ISB IF OUT J9 Connector (Optional)

This rear panel connector provides access to the ISB IF signal when the Receiver is in the ISB mode (if the ISB option (A5) is installed). The J9 connector will mate with any standard male BNC-type connector.

2.3.1.7 A6A1W1J1 Remote Control Interface (Optional RS232C/MIL-STD-188C)

This connector is a round, 26-pin MIL-Type M38723-02R-1626N and permits the Receiver to be operated from a remote control device. A mating connector is supplied. Depending on which interface is required, pin connections, jumper options and baud rate selection must be appropriately set. (Refer to Paragraphs 2.3.4 and 2.3.4.6, Receiver System Connections.)

2.3.1.8 INT EXT S2 Slide Switch

Setting this switch to the INT position selects the internal time base for the Receiver and provides an internal 1 MHz reference output at connector J7. Setting the switch to the EXT position deactivates the internal reference so that an external signal may be applied to J7. The Receiver is normally shipped from the factory preset for a 1 MHz reference; however, provision for changing to 5 MHz or 10 MHz is available by changing links on the A8 assembly. (Refer to Paragraph 2.3.4.5).

2.3.1.9 GROUND Lug

A GROUND Lug is located at the lower right corner of the receiver rear panel. Ensure that adequate grounding techniques are employed when operating, installing options and performing maintenance functions on the RA6793A Receiver.

2.3.1.10 PHONES Jack

This output is intended to drive a 600 ohm headphone set and provides an audio output from the Receiver in all operating modes.

2.3.2 Installation Options

The available options associated with the Receiver are detailed in Paragraph 1.4. One or more of the filters must be installed before the Receiver can operate. The ISB capability, however, is optional. Because of the different possible filter combinations and the options, it is recommended that a receiver configuration chart or log book be maintained for each Receiver. The configuration chart or log book should list the IF bandwidth filters currently installed in the Receiver, the operating options, and the type of remote control interface, as examples.

In addition, an internal option of operating the RA6793A Receiver with a 1, 5 or 10 MHz reference is available by changing links on the A8 assembly.

2.3.3 RA6793A Receiver Options Installation Procedures

The installation procedures for the Receiver may be logically divided into three steps: (1) installation of the primary operating options to include the plug-in filters and independent sideband; (2) making the required system connections; and (3) installation of the Receiver in an operational position. Paragraph 2.3.3.1 through 2.3.4.6 detail the installation steps necessary for preparing the RA6793A HF Receiver for operation. Figure 2-4 thru 2-6 are photographs of the details associated with installing the Receiver operating options.

2.3.3.1 Optional IF Bandwidth Filters

The standard RA6793A HF Receiver is supplied with soldered-in mechanical filters and input and output shunt capacitors. If conversion to plug-in filters is desired for receivers not originally supplied with any other optional filters, the removal of the mechancial filters and capacitors should be performed at the RCI factory.

The Receiver may be supplied with from 1 to 7 plug-in filters. Table 2-1 lists the optional filters available with the initial procurement. Mounted on the A4 board, the filters are accessible from the top of the Receiver. To gain access to the A4 board, loosen the six quarter-turn fasteners holding the top cover to the Receiver and carefully remove the top cover. An RF shield is mounted over the filter sockets on the A4 board. Remove the three screws holding this shield to the chassis and remove the shield. Figure 2-4 illustrates the seven filter slots on the A4 board.

If a Receiver configuration chart has been prepared for this particular Receiver, refer to the chart and determine if the Receiver is to be operated with the ISB option. If the receiver configuration chart was not prepared, determine if the ISB option is to be included by checking the shipping data. When operating with the ISB option, both upper and lower sideband filters must be installed in the Receiver, and the lower sideband filter must be installed in the FL1 position. If the ISB option is not used, either a lower sideband filter or symmetrical sideband filter may be installed in the FL1 position. When a lower sideband filter is installed, the companion upper sideband filter must be installed in one of the remaining filter positions. If a symmetrical sideband filter is used, the Receiver will use the filter installed in the FL1 position for both sidebands by making the approprite frequency offsets to the first and last local oscillators. The remaining filters may be installed in any sequence in filter positions FL2 through FL7. However, in order to simplify system operation and troubleshooting, it is recommended that a format be established and used for all Receivers at a particular site.

Once the filter complement and arrangement has been determined, the following procedure should be used to insert the plug-in filters into the Receiver. Refer to Figures 2-4 and 2-5.

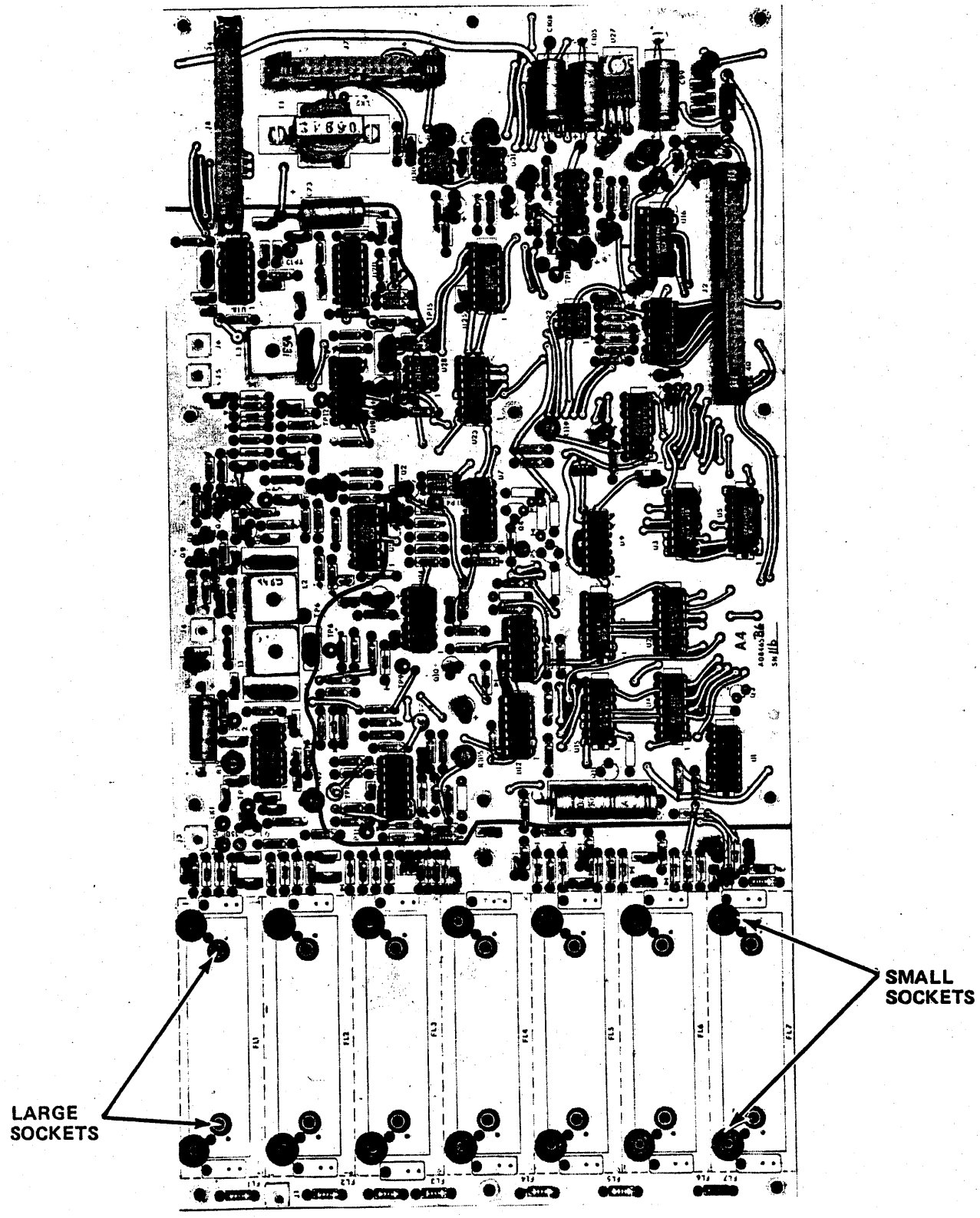


Figure 2-4. Location of IF Bandwidth Filter Slots

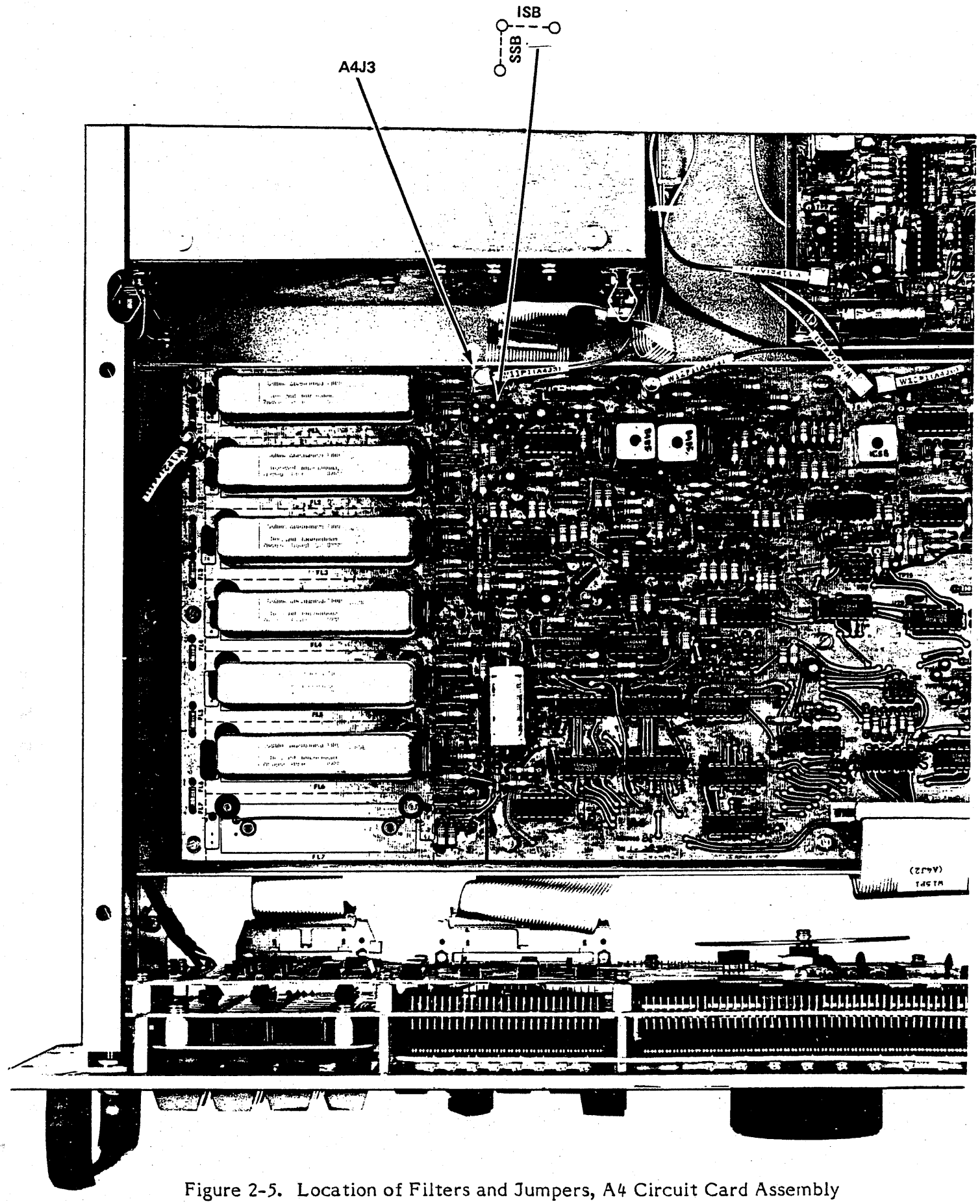


Figure 2-5. Location of Filters and Jumpers, A4 Circuit Card Assembly

1. Working from the front of the Receiver, position the filter to be used for LSB operation over filter position FL1 (the filter position closest to the rear of the Receiver). Make certain that the large pins are aligned with the large sockets and the smaller pins are aligned with the smaller sockets.
2. Carefully push down on the filter to insert the pins into the sockets. Relatively light pressure is required to insert the pins into the sockets. If the filter does not easily slide into place, recheck the pin/socket alignments.
3. Insert the appropriate filters into filter positions FL2 through FL7 (as required), using the procedures described in steps 1 and 2.
4. After all filters have been inserted, visually inspect the filters to ensure that they are properly seated. The bottom of the filters should be flat against the surface of the A4 board.
5. Replace the RF shield over the filters and secure the shield in place by tightening the three screws.

NOTE

If the Receiver is to be equipped for operation in the ISB mode, continue with the procedures described in Paragraph 2.3.3.2. If the Receiver is not to be equipped with this option, replace the top cover on the receiver chassis, and proceed to Paragraph 2.3.3.3, Line Level Adjustments.

Table 2-1. RA6793A Optional Bandpass Filter List

BANDWIDTH	DESCRIPTION	SHAPE FACTOR 3 dB:60 dB	DIFFERENTIAL DELAY uS	RACAL NUMBER
*0.3 kHz	Symmetrical BPF	1:6.7	-	07883-1
*3.2 kHz	Symmetrical BPF	1:2.7	-	07883-3
*4.0 kHz	Symmetrical BPF	1:2.5	-	3600001
*5.0 kHz	Symmetrical BPF	1:2.5	-	3600002
*6.0 kHz	Symmetrical BPF	1:2.3	-	07883-4
*450 Hz to 3000 Hz	ISB/USB BPF	1:1.92	-	07883-5
*450 Hz to 2700 Hz	ISB/LSB BPF	1:1.92	-	07883-6
*350 Hz to 2700 Hz	USB BPF	1:1.66	-	08669
*300 Hz to 2200 Hz	USB BPF	1:1.97	-	08771
1.0 kHz	Symmetrical BPF	1:6	25	3600003
3.0 kHz	Symmetrical BPF	1:6	13	3600004
6.0 kHz	Symmetrical BPF	1:6	10	3600005
1.0 kHz	Symmetrical BPF	1:2.5	1080	3600006
3.0 kHz	Symmetrical BPF	1:2.5	360	3600007
6.0 kHz	Symmetrical BPF	1:2.5	180	3600008
0.125 kHz	Symmetrical BPF	1:5.33	-	08699
0.4 kHz	Symmetrical BPF	1:6.2	-	08406
1.2 kHz	Symmetrical BPF	1:6	-	08407
6.8 kHz	Symmetrical BPF	1:3.3	-	08408
350 Hz to 3050 Hz	ISB/LSB BPF	1:1.6	800	08409
350 Hz to 3050 Hz	ISB/USB	1:1.6	800	08410
0.4 kHz	Symmetrical BPF	1:2.5	2000	08411

BANDWIDTH	DESCRIPTION	SHAPE FACTOR 3 dB:60 dB	DIFFERENTIAL DELAY uS	RACAL NUMBER
1.2 kHz	Symmetrical BPF	1:2	1000	08412
3.24 kHz	Symmetrical BPF	1:1.33	1000	08413
6.8 kHz	Symmetrical BPF	1:2	1000	08414
16.0 kHz	Symmetrical BPF	1:2	40	08415
0.5 kHz	Symmetrical BPF	1:6	80	08416
1.0 kHz	Symmetrical BPF	1:6	40	08417
2.0 kHz	Symmetrical BPF	1:6	20	08418
3.0 kHz	Symmetrical BPF	1:6	20	08419
6.0 kHz	Symmetrical BPF	1:6	20	08420
0.075 kHz	Symmetrical BPF	1:6.67	-	08589

*Mechanical filters all other are Crystal filters.

2.3.3.2 Indpendent Sideband (ISB) (Optional)

If the Receiver is to be operated in the ISB mode, the A5 circuit card assembly must be installed in the Receiver. The A5 card is located towards the rear of the Receiver, between the A1 assembly and the A4 circuit card assembly as shown in Figure 2-6. The following procedure details the steps necessary to install the A5 circuit card assembly. Refer to Figures 2-5 and 2-6 for the location of cables and connectors.

1. Place the metal baseplate shield (curved edge upwards) on the four standoffs and secure with four screws through the standoffs.
2. Position the A5 circuit card assembly so that the ribbon cable is near the J8 connector on the A4 circuit card assembly. Secure the A5 circuit card assembly to the metal baseplate with 4 screws.
3. Plug in the ribbon cable (A5W1) from the A5 card into J8 on the A4 board. Connect coaxial cable W10 between A4J6 and A5J3. Connect coaxial cable W11 between A4J3 and A5J1.
4. The mechanical jumper on the A4 circuit card assembly must be properly positioned for ISB/SSB operation. The jumper, designated LK1, is physically located to the right of filter position FL1 when looking from the front of the Receiver, (Refer to Figure 2-5.) With the A5 circuit card assembly installed, the jumper must be connected across the two terminals designated ISB.

NOTE

Upon completing all required installation options procedures, it is recommended that the Line Level Adjustment procedure be performed as outlined in Paragraph 2.3.3.3. Upon completing this adjustment procedure, the RA6793A Receiver Options Installation Check as described in Section III, Paragraph 3.3.1 should be performed. After completing this operational check, it is suggested that the System Connections check be made in accordance with the procedures listed in Paragraph 2.3.4 through 2.3.4.6.

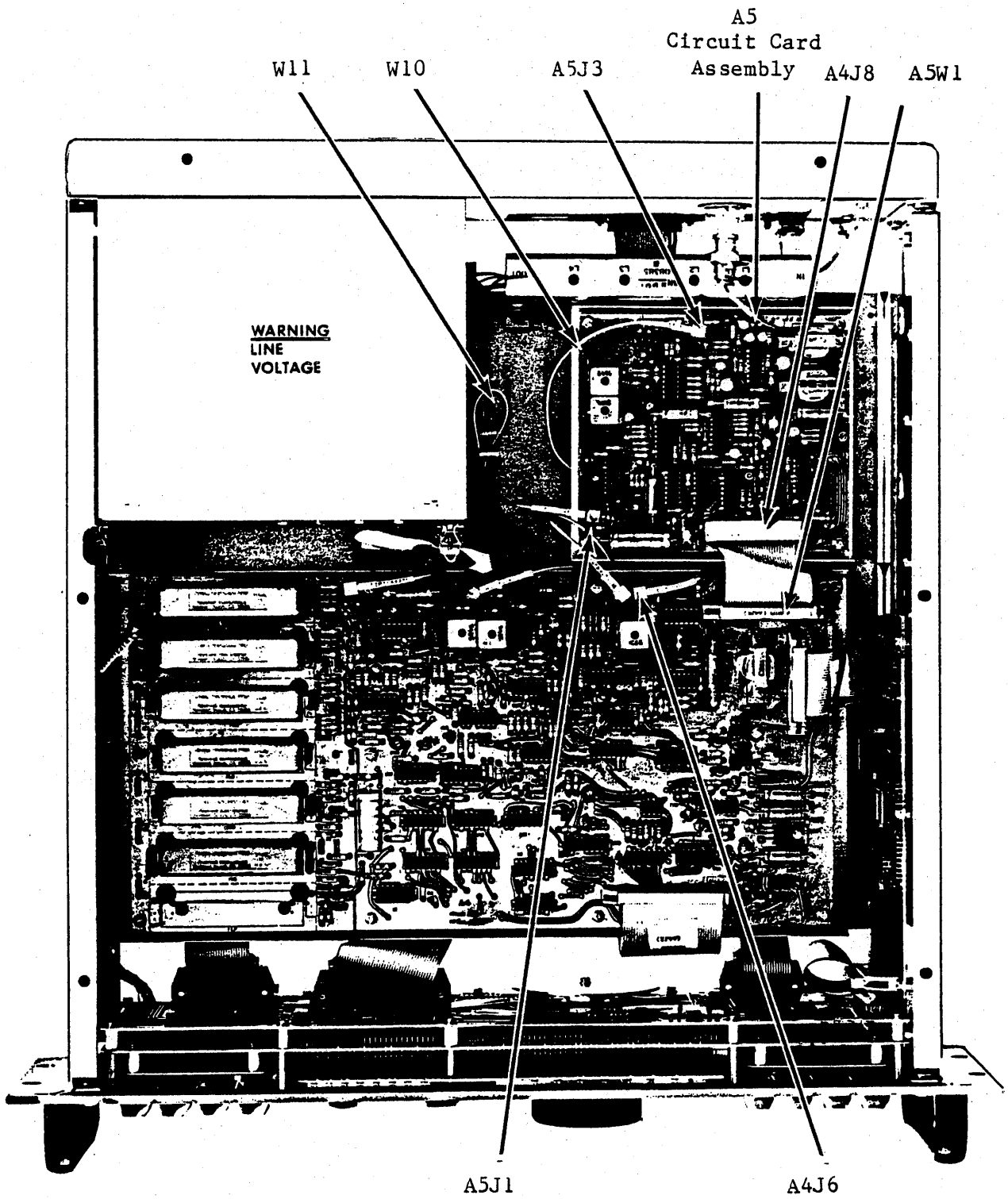


Figure 2-6. Receiver Options, Installation Details

2.3.3.3 Line Level Adjustments

The following procedures are detailed for adjustment of the audio line level, required upon installation of the receiver.

1. For MAIN LINE LEVEL Adjustments:

   a. Set the following controls as indicated:

POWER switch	ON
AGC	SHORT
METER switch	AF
MODE	AM (depress AM pushbutton switch on lefthand keypad until the word AM is displayed under the word MODE in the Mode LCD).
BW	Approximately 6 kHz

   b. Connect the AM output (with modulation set for 30%) from an RF signal generator (HP8640, or equivalent) set to a frequency of 3.50000 MHz and an output of -97 dBm, to the RF IN connector J1 on the rear panel.

   c. Set the receiver frequency to 3.50000 MHz.

   d. Using a screwdriver, adjust the MAIN LINE LEVEL potentiometer on the receiver front panel for 1 mW audio output level, as indicated by the 0 dB line on the AF meter scale in the Mode LCD.

   e. Turn POWER switch to off and disconnect the generator.

2. For I-LSB LINE LEVEL Adjustment (requires ISB optional fitting):

   a. Set the following controls as indicated:

POWER switch	ON
AGC	SHORT
METER switch	AF
MODE	I-LSB (depress ISB U/L switch once or twice until the I-LSB word is displayed under the word MODE in Mode LCD).

   b. Connect the CW output from an RF signal generator (HP8640, or equivalent) to a frequency of 3.50000 MHz and an output of -97 dBm, to the RF IN connector J1 on the rear panel.

   c. Set the receiver frequency to 3.501800 MHz

   d. Using a screwdriver, adjust the I-LSB LINE LEVEL potentiometer on the receiver front panel for a 1 mW audio output level, as indicated by the 0 dB line on the AF meter scale in the Mode LCD.

NOTE

The USB line level was adjusted when the MAIN LINE LEVEL was set since the USB AF uses the main AF channel when the receiver is in the USB mode.

e. Turn POWER switch to off and disconnect the generator.

2.3.4 RA6793A Receiver System Connections

System connections for the receiver are based on the individual site requirements and the options associated with a receiver. The site requirements will determine the most effective method of installation. In some installations, it may be easier to pre-wire an entire equipment rack and then install the receiver. In others, it may be easier to install the receiver and then add the wiring. The following paragraphs detail the procedures associated with installing the receiver. Figure 2-7 illustrates the connectors located on the rear panel of the receiver.

2.3.4.1 Power Input Connections

A three-conductor power cord is supplied with the Receiver for connection to the power input plug. The connector has the following pin assignments, as viewed from the rear panel:

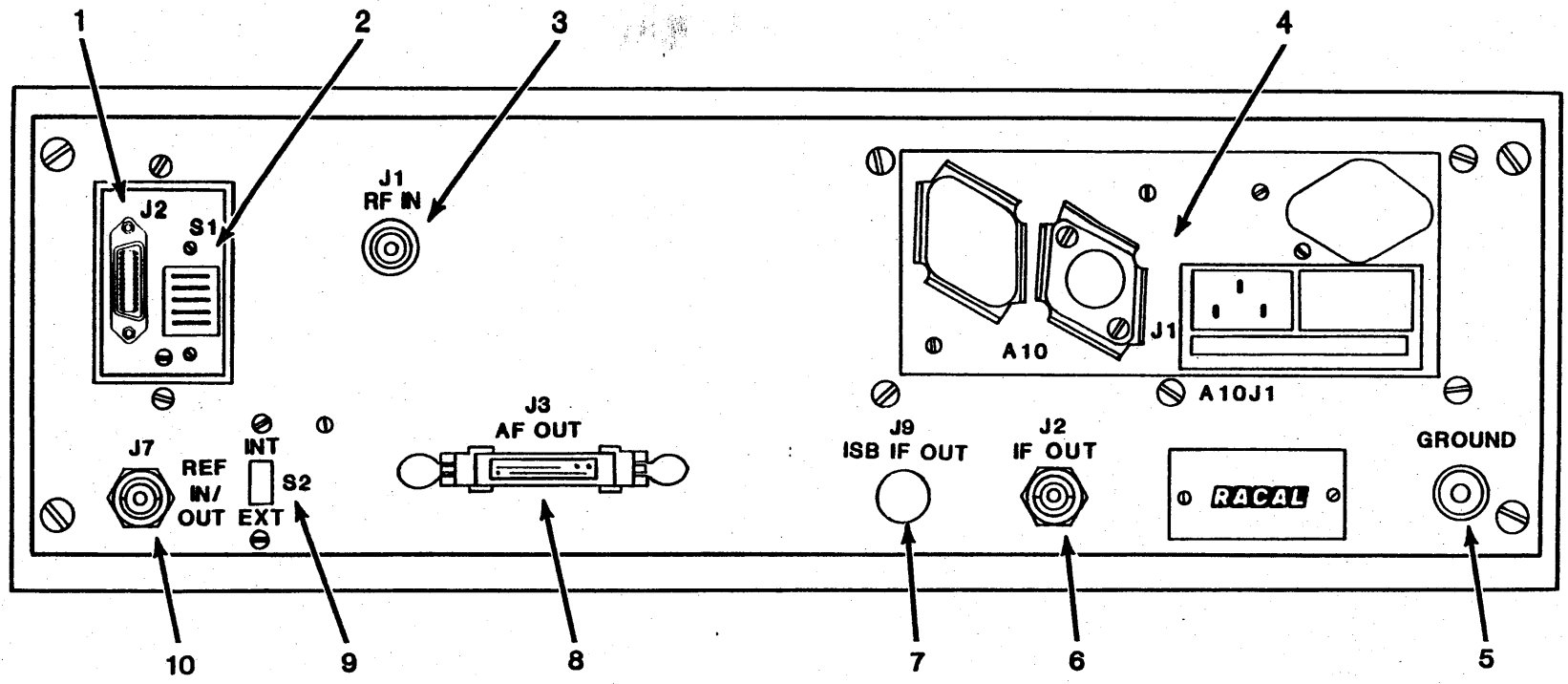
Left Pin:	LINE
Center Pin:	GROUND
Right Pin:	NEUTRAL

With the power cable unplugged from the receiver, the clear plastic window can be slid over the three male power receptacle prongs. This exposes the line fuse and a hinged, plastic FUSE PULL lever. If the voltage shown does not match the available line voltage, remove the pc wafer and reinstall it so that the line voltage closest to the available line voltage is visible with the pc wafer in position. Install the fuse suitable for the line voltage: 1 amp slow-blow for 100 V ac and 120 V ac, or 1/2 amp for 220 V ac and 240 V ac. (An extra fuse may be installed in the alternate fuse holder, XF2 which is located internally on the A10 Power Supply Assembly.) Slide the clear plastic window back over the fuse and pc wafer portion of the fuse holder assembly and insert the power cable, W18, in the receptacle. Additionally, the receiver should be grounded by attaching a suitable ground wire to the rear panel GROUND lug before the power cable, W18, is attached.

The Receiver is normally shipped from the factory configured for operation with a 120 volt, ±10%, 48 to 420 Hz ac source. For receiver operation with a 240 volt source, the receiver must be re-configured as follows:

1. Disconnect the receiver from all system equipment and remove the power cord.

2. On the power input connector assembly A10J1: Slide the transparent protective cover to the left to expose the fuse; remove the fuse; remove the printed circuit wafer, and then replace the wafer with the required nominal



1. Remote Control Interface Connector (A6A1J2)
2. Address Switch Assembly (A6A1S1)
3. RF IN Connector (J1)
4. AC Power Input Connector
5. GROUND Terminal
6. IF OUT Connector (J2)
7. ISB IF OUT Connector (J9)
8. AF OUT Connector (J3)
9. INT/EXT Reference Frequency Selector Switch (S2)
10. REF IN/OUT Frequency Connector (J7)

Figure 2-7. Rear Panel Systems Connection

operating voltage visible; replace the fuse and restore the protective cover to its original position and connect or re-connect the receiver system connections.

3. The unit is now ready for operation from the selected line voltage.

CAUTION

The supply voltage should remain with 10% of the selected terminal voltage. A lower voltage can cause the internal regulation circuits to trip and a higher voltage can cause excessive internal temperatures.

2.3.4.2 RF Input Connector (J1)

The Receiver is shipped with a plastic dust cover over connector J1 which must be removed before the antenna connection can be made. Ensure that a suitable antenna is selected. The input impedance at the connector is 50 ohms, Unbalanced with VSWR of 2:1.

2.3.4.3 IF Output Connector (J2)

The IF Output Connector J2 located on the rear panel is shipped with a plastic dust cover which must be removed before connection. During operation, a 455 kHz IF frequency is supplied at this connector for connection to external equipment. Nominal level is -10 dBm into 50 ohms.

2.3.4.4 AF Output Connector (J3)

A mating connector (Cannon type DB-25P) with a connector shell is supplied with the Receiver. Use the following procedure, and pin number/signal designation information in Table 2-2 to wire the connector.

1. Slide the connector shell over the cable to be used.

2. Solder the cable wires to the connector as required (refer to Table 2-2). The connector pin numbers are indicated on the front of the connector.

3. Slide the connector back into the connector shell. Place one of the spring clips on top of the connector with the curved edge pointing upwards. Secure the spring clip and the connector to the connector shell with the self-tapping screw. Repeat this procedure for the other side of the connector.

4. Connect the wired cable to the rear panel connector J3 and secure with two connector springs.

Table 2-2. AF OUT J3 Pin Connections

Pin Number	Signal Designation	
1 2 14	Output Center Tap Output	Line 1 Output (used only with ISB Option). Provides USB output during ISB operation; AM/FM/CW/SSB output during non-ISB operation.

Table 2-2. AF OUT J3 Pin Connections (Cont.)

Pin Number	Signal Designation	
3 16 15	Output Center Tap Output	Line 2 Output (Used only with ISB Option). Provides LSB output during ISB operation.
4 5 17	Output Center Tap Output	Monitor Line Output. Provides AM/FM/CW/SSB output during non-ISB operation; provides switch controlled selection of USB or LSB during ISB operation.
18 6	Output Signal Ground	Loudspeaker Output. Same as Monitor Line Output.
7,8,9 10,11,12,13, 19,20,24,25	Ground Not Connected	
20	Mute Control (Used with RF Preamp Option 08076-2)	
21	Main IF Diversity AGC Monitor/Input	
22	ISB Lower Sideband Diversity AGC Monitor/Input	
23	Fault Indicator (Low indicates Fault)	

2.3.4.5 Reference Input/Output Connector (J7)

This BNC-type connector is used in conjunction with the INT/EXT S2 slide switch to accept an external reference source or provide an output of the internally generated reference signal. The reference frequency is generated by a oven controlled crystal oscillator (OCXO) located on circuit card A8, or by a frequency source external to the Receiver. The Receiver is normally shipped from the factory with a preset 1 MHz reference. Provision is made, however for compatibility with a 5 or 10 MHz source through internal linkage on the A8, 2nd LO/BFO Synthesizer Board.

After determining the frequency source compatibility requirements, refer to Table 2-3 and make the following link changes on the A8 circuit board if required.

1. For 1 MHz operation, LK1 and LK2 are fitted (E1 to E2, and E3 to E4 respectively).

2. For 5 MHz operation, LK2 ONLY is fitted (E3 to E4).

3. For 10 MHz operation, LK1 ONLY is fitted (E1 to E2).

Table 2-3. External/Internal Link Options

Frequency Source Selection	
1 MHz	Connect LK1 and LK2
5 MHz	Connect LK2
10 MHz	Connect LK1

Upon completing the required link changes, ensure that switch, S2 INT/EXT located on the rear panel is set in the appropriate position.

2.3.4.6 Remote Control Serial Asynchronous Interface Connections (A6A1W1J1)

The Receiver is supplied with a mating connector for the remote control interface connector. Figure 2-8 illustrates the pin designations and assigned functions. The pins designated A through J vary in function according to the interface being used, as is shown in Table 2-4. The remaining pins K through C are the same for all the listed interfaces. Table 2-5 lists the baud rate selection bit associated with pins W through Z for different data rates (baud) selection. Table 2-6 lists the required link configurations on the A6A1 circuit card assembly for the different interfaces.

To make the required connections:

1. Slide the mating connector shell over the cable to be used for the remote control.

2. Solder the wires to the appropriate connector pins in accordance with Figure 2-8 and Tables 2-4 and 2-5 for the interface to be used. The connector pins are designated on the front of the connector.

3. After carefully checking all wiring, slide the connector into the connector shell and secure the cable clamp. Attach and secure the connector to A6A1W1J1.

4. Visually inspect the A6A1 circuit card assembly to insure that all jumpers are installed in accordance with Table 2-6.

NOTE

The MIL-STD-188C and RS-232C interfaces are electrically compatible. The distinction between the two is the polarity definition for "MARK" or "LOGIC 1". RS-232C defines "MARK" as a negative potential while MIL-STD-188C defines "MARK" as positive. Therefore, pin functions (Figure 2-12, Table 2-5) marked DATA IN A/DATA OUT A are "MARK" negative and DATA IN B/DATA OUT B are "MARK" positive.

Table 2-4. Data Connection Interface Compatibility

J1 Pins	MS188C	RS232C - RS423	RS422
A	System Gnd	System Gnd.	System Gnd.
B	Not Used	Data Out A	Data Out A
C	Data Out Gnd.	Dat Out Gnd.	Not Used
D	Data Out	Not Used	Data Out B
E	Jumper to 'F'	Not Used	Not Used
F	Jumper to 'E'	Data In 'A'	Data In 'A'
G	Data In Gnd.	Data In Gnd.	Not Used
H	Data In	Jumper to 'J'	Data In 'B'
J	Not Used	Jumper To 'H'	Not Used

Table 2-6. A6A1 Link Configurations

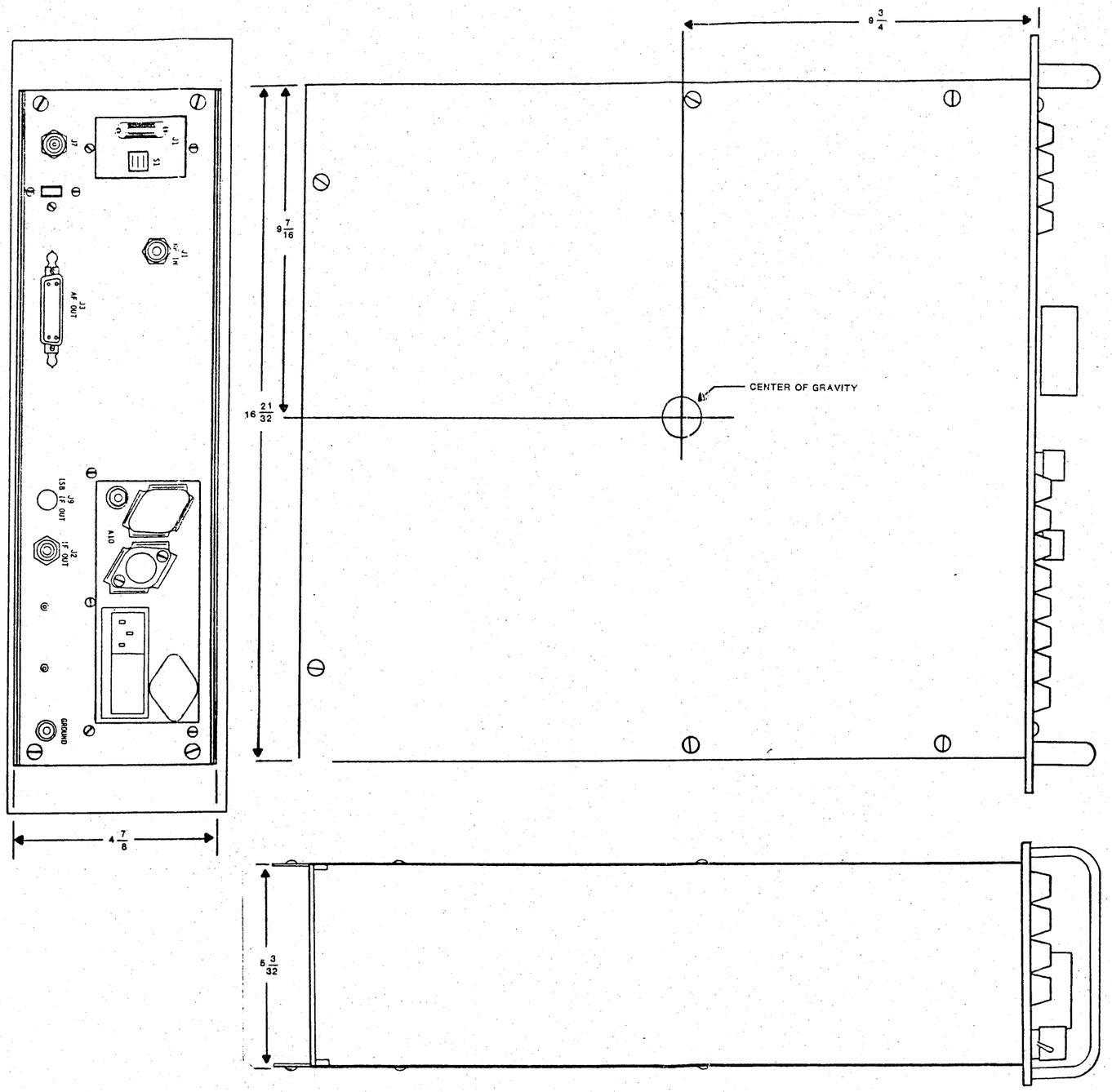
Link No.	188C/232C/423	422
LK1	Install	Install
LK2	Remove	Remove
LK3	Install	Remove
LK4	Install	Remove
LK5	Install	Remove
LK6	Remove	Install

Table 2-7. Parity Select

No Parity	High	Open
Parity	Low	Ground
Even	High	Open
Odd	Low	Ground

Table 2-5.
Interface Connector
Baud Rate Selection

Data Rate Selection Bit				Data Rate
W	X	Y	Z	(Baud)
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1,200
1	0	0	0	1,800
1	0	0	1	2,000
1	0	1	0	2,400
1	0	1	1	3,600
1	1	0	0	4,800
1	1	0	1	7,200
1	1	1	0	9,600
1	1	1	1	19,200



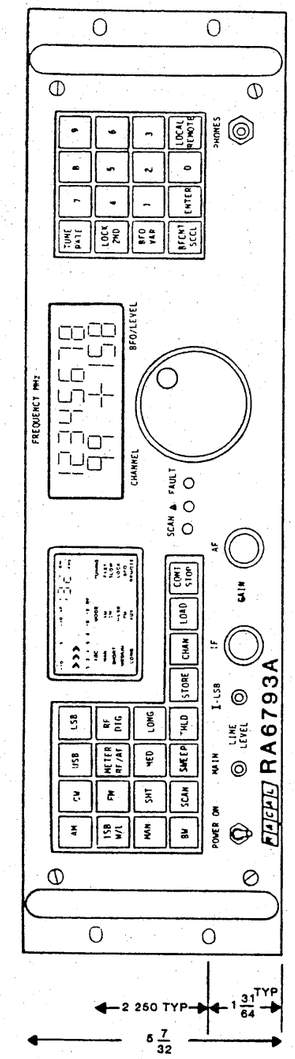


Figure 2-1. RA6793A HF Receiver, Installation Drawing

SECTION III
OPERATION

3.1 GENERAL INFORMATION

All front panel controls, displays and indicators (Figure 3-1) are described in Paragraphs 3.2 through 3.2.11. Detailed operating procedures are presented in Paragraphs 3.3 through 3.3.3.2 in a logical sequence. After performing an operating check and upon completion of any required system interface connections (SECTION II, Paragraphs 2.3.4 through 2.3.4.6), a Receiver/System Interface Check (SECTION III, Paragraph 3.3.2) should be performed which will provide verification of all system connections.

3.2 FRONT PANEL CONTROLS, DISPLAYS/INDICATORS

3.2.1 POWER-ON Toggle Switch

A double pole, single-throw toggle switch provides on-off control for the Receiver by controlling the primary power source to the power supply. During initial installation, be sure the line-voltage-select pc wafer on the rear panel matches the available line voltage before energizing the Receiver. Refer to SECTION II, Paragraph 2.3.4.1 for the voltage selection procedure.

3.2.2. Manual Tuning Knob

Optically coupled to a tuning encoder, the tuning knob provides selection of receiver operating frequency or BFO frequency. (Refer to TUNE RATE and BFO/BFO CENTER pushbutton controls.) The rate of change of the frequency depends on the speed the tuning knob is rotated and the rate of tune selected through the TUNE RATE switch. Clockwise rotation increases the frequency, counterclockwise rotation decreases the frequency. Continuing to tune past the end of the range causes the receiver to step to the opposite end of band and to continue tuning in the same increasing or decreasing frequency direction. Additionally, whenever the channel display is illuminated and the Receiver isn't scanning, the manual tuning knob will increment or decrement the channel number at the rate of ten channels per turn.

3.2.3 IF GAIN Potentiometer

This front panel control is used to establish the receiver overall gain when the Receiver is operated in the manual mode, and to set the threshold level when the Receiver is operated in the automatic mode with a manually set threshold. Clockwise rotation increases IF signal (overall gain) level, while counter-clockwise rotation decreases IF signal (overall gain) level. This control affects the IF signal level output through IF OUT connector J2, and the audio outputs through J3.

3.2.4 AF GAIN Potentiometer

This front panel control is used to control the level of the receiver audio outputs. Clockwise rotation of the potentiometer increases loudness of the audio signal to the PHONES jack and the external L/S output located on the AF Out Connector J3, while counterclockwise rotation decreases loudness.

3.2.5 MAIN LINE LEVEL Screwdriver-Set Potentiometer

This potentiometer is used to adjust the line level when the Receiver is operated in the AM, FM, CW, or SSB modes. If the Receiver is equipped to operate in the ISB mode (optional A5 circuit card assembly is installed), this control will adjust the line level of the upper sideband.

3.2.6 I-LSB LINE LEVEL Screwdriver-Set Potentiometer

This potentiometer is used to adjust the line level of the lower sideband when the Receiver is operated in the ISB mode (optional A5 assembly installed).

3.2.7 Leftside Pushbutton Switches

a. Detection Mode: AM, CW, USB, LSB, ISB U/L, FM.

These pushbuttons are used to select the operating mode of the Receiver. (Refer to SECTION I, Figure 1-2.) The ISB U/L will be enabled only if the Receiver is equipped with the ISB option. If the Receiver is equipped with this option, depressing the pushbutton will activate both the USB and LSB channels simultaneously. If the front panel display indicates I-USB, the PHONES jack will be connected to the upper sideband channel. Depressing ISB U/L a second time will change the display and connect the PHONES jack to the LSB channel. The monitor line and loudspeaker outputs, through rear panel connector J3, will also be switched with the ISB U/L pushbutton switch.

b. Bandwidth Pushbutton Switch: BW

This pushbutton key-switch is used to select specific IF bandpass filter bandwidths within the modified receiver. The modified receiver is capable of accepting up to seven plug-in IF bandpass filters and operating with up to five symmetrical filters. The upper/lower sideband filters will automatically be used when the USB or LSB detection mode is selected. The remaining filters (up to total of five) are selected by scrolling through the progressively higher bandwidths by depressing the BW pushbutton key-switch.

c. METER RF/AF Pushbutton Switch

This pushbutton switch is used to change the front panel meter display to either an RF scale or and AF scale. The Receiver will always display either scale. Depressing the pushbutton will cause the display to switch either from RF to AF or AF to RF.

d. Gain Mode Pushbutton Switches: MAN, SHORT, MED, LONG

The Receiver is designed to operate with three different gain control modes: Manual, Automatic, and Automatic with a selectable threshold. Depressing the MAN pushbutton switch causes the MAN indication to appear in the display. If an automatic indication (SHORT, MEDIUM, or LONG) is present in the display, it may be deleted by depressing the corresponding pushbutton switch. The Receiver is now in the manual mode with gain control under the front panel IF GAIN control. When the Receiver is switched out of the manual mode, it will automatically enter the SHORT AGC mode. The medium or long AGC modes may be selected by

depressing the corresponding pushbutton switches. The AGC mode with a manually set threshold is enabled by depressing an AGC mode pushbutton switch while in the manual mode. The MAN pushbutton switch is the push-on/push-off type. In the manual mode, the AGC pushbutton switches are push-on/push-off, while in the automatic mode they are push-on.

e. STORE

This pushbutton switch allows data displayed on the front panel of the Receiver to be stored in any of the 100 available channels. Pressing and holding STORE allows channel number selection through the use of the numerical digit pushbuttons. The channel number displayed when STORE is released is the channel that Receiver parameters currently set in the Receiver will be stored in.

f. LOAD

This pushbutton operates only when the Receiver is in the "Delta Mode" (Delta indicator lit), and causes the data displayed in the Delta Mode to be transferred to the Receiver. When depressed and released, Load causes (1) both the Receiver and Receiver displays to be updated; (2) the Receiver to be left in "Receiver Mode", and (3) the Delta indicator to be off.

g. SCAN

This pushbutton has three functions: (1) setting the scan flag; (2) beginning or resuming cell scan; and (3) stopping cell scan. When the Receiver is in the Delta Mode, pressing SCAN alternately lights and extinguishes the SCAN indicator. If the SCAN indicator is lit for any given channel then the scan flag is set for that channel and the channel will participate in the cell scan. If the indicator is off the scan flag is not set and channel will not participate and will be skipped during cell scan. When in the Receiver Mode (Delta indicator off), pressing SCAN begins or resumes the cell scan. Pressing SCAN again stops the scan. SCAN may be resumed at any time from the current channel as long as a channel number is present in the channel display.

h. CHAN

When pressed, this pusbutton toggles from Receiver Mode (Delta indicator off) to Delta Mode (Delta indicator on). Each of these modes offers a channel preview capability: in the Receiver Mode, as a channel is selected the channel settings (parameters) are displayed and the Receiver tunes to the parameters. In the Delta Mode, the information stored in any selected channel is presented on the displays without altering the current parameter settings in the Receiver. After pressing CHAN which causes the Receiver to enter Delta Mode, pressing two numerical pushbuttons will select a new channel number.

i. RF DIG

Pressing and holding this pushbutton key-switch causes the BFO/LEVEL LCD display to indicate signal level. This level should not be equated in dBm. A 00 selection represents minimum attenuation (max gain), whereas, a 150 selection represents maximum attenuation (minimum gain). In addition, this control is used to determine the incoming signal level when setting the system threshold for scan and scan and sweep mode halt (stop on signal) functions.

j. THLD

This pushbutton key-switch functions as a push-on/push-off type control, which is used to select the BFO display and indicate the stop-on signal threshold level to be set for loading into a channel storage location in conjunction with other modes. If the channel is used in a cell scan, this threshold will be used by the modified receiver to instigate a scan halt condition if the incoming signal exceeds the set threshold level.

To set the threshold, press the THLD pushbutton key-switch so that the BFO/LEVEL LDC display shows a signal level. To alter the level, press ENTER to clear the last stored value and then enter a number from 0 to 150, using the numerical pushbutton key-switches. An out-of-range entry is indicated by three dashes in the display. To store this value in a channel, use the store mode in the normal way.

NOTE

To review the threshold level set in any channel, use the channel (CHAN) review mode and select the threshold mode.

k. SWEEP

This pushbutton key-switch is used to initiate the sweep mode, following a loading of set-up conditions from the channel storage area. To use the sweep mode, three upward consecutive channel storage locations must be loaded as follows:

Location 1: All initial conditions including threshold (if required) and start point frequency.

Location 2: Stop point or roll-over frequency.

Location 3: Frequency indicating step size.

To initiate sweep mode, use the channel (CHAN pushbutton key-switch) mode to load the contents of location 1, then press the SWEEP pushbutton key-switch. The SCAN LED will illuminate and the display should show the frequency progress in an upward direction. If sweep function fails to start, it may be that the last rate selected through actuation of the numerical pushbutton key-switches was 0 (zero). This means that it will be necessary to press a numeric pushbutton key-switch from 1 through 9 to begin the sweep function; pressing 1 allows the fastest step rate and can be slowed down by progressively selecting numerals 2 through 9.

To disable the sweep mode, press SWEEP pushbutton key-switch once again.

l. CONT-STOP

This pushbutton key-switch is used in the secondary function sweep and scan modes to continue from a stopped-on-signal condition. The CONT-STOP pushbutton key-switch is also used in the stop function to enable the secondary function sweep and scan modes. To access the secondary function modes, press LOCK-2ND pushbutton key-switch and CONT/STOP simultaneously, then hold down for approximately one-

second and the AUX indicator on the LCD mode display will illuminate. The modified receiver is now set to stop on signals that exceed the threshold set in each stored channel location.

When the modified receiver is actually stopped following a signal/threshold decision, the SCAN LED will flash until the CONT-STOP pushbutton key-switch is pressed, which allows continuation from this halted condition.

NOTE

In the sweep mode, numeric pushbutton key-switches 1-9 function as a speed pad; key-switch 1 providing 25 milliseconds per step, and 9 providing 10 seconds. Pushbutton key-switch 0 is used to pause to sweep.

3.2.8 Rightside Pushbutton Switches

a. TUNE RATE

Provides for fine (1 Hz increments), slow (30 Hz increments) and fast (1 kHz increments) selection of receiver operating frequency through rotation of the Manual Tuning Knob.

b. Numerical Pushbutton Switches 0 through 9 and ENTER

The first function of the numerical switches is to set the Receiver to a particular operating frequency. Depressing the ENTER pushbutton switch will enable the numeric keys. The first numeric key depressed will be recognized by the Receiver as the ten's MHz digit. Since the Receiver cannot be tuned above 29.999999 MHz, the Receiver will recognize only 0, 1, or 2 as the first digit entered.

The second numeric key depressed will be recognized as the units' MHz digit with the third numeric key depressed as the hundreds' kHz digit.

The second function of the numerical pushbuttons is to select a channel. Depressing two digits after pressing CHAN will select a new channel number. The third function of the numerical switches is to select channel dwell time when the Receiver is in the Scan Mode. The dwell time is selected by pressing one of the numerical buttons from 0 through 9. "0" selects a dwell time of approximately 10 seconds. "1" through "8" select intermediate rates from short to long respectively. The dwell time may be changed at any time during Scan Mode by pressing another numerical button.

c. LOCK - 2ND

This pushbutton switch is the push-on type. When the lock mode is activated, as indicated by the word LOCK in the display, the front panel tuning knob will be disabled. The lock mode is disabled by depressing the TUNE RATE pushbutton switch. The "2nd" function is used to enter secondary operation modes. (See descriptions on SWEEP and SCAN).

d. BF/CNT-SC CLR

This pushbutton key-switch, when depressed in the CW mode, will reset the BFO offset frequency to zero (0). Depressing the pushbutton key-switch a second time will return the BFO to the previously selected frequency. When used in conjunction with the LOCK-2ND mode function, depressing this pushbutton key-switch will clear all previously set scan flags in the modified receiver.

e. LOCAL/REMOTE

The push-on/push-off type pushbutton switch will set the Receiver to operate either in the LOCAL operating condition (control of the Receiver is through front panel) or the REMOTE operating condition. Note that the Receiver must be equipped with the A6A1 Remote Control Interface Circuit Card Assembly to be operated in the remote control condition.

3.2.9 Left (Mode/Meter) Liquid Crystal Display (LCD)

a. -10 0 +10 AF
0 2 4 6 8 10 12 RF

Located in the upper left corner of the Mode/Meter LCD, the meter display indicates audio level in dBm (when AF selected), and RF in uV (when RF selected). The scale is selected through the METER RF/AF BW pushbutton switch.

b. BW kHz

Located in the upper right corner of the Mode/Meter LCD, the BW kHz display indicates the IF bandwidth selected through depressing the BW pushbutton switch from one to five times to correspond with BW1 through BW5.

c. AGC
MAN
SHORT
MEDIUM
LONG

Located in the lower left corner of the Mode/Meter LCD, the word AGC is always present. The word MAN will be present when the Receiver is being operated in the manual gain control mode. Under the word AGC, the words SHORT, MEDIUM or LONG when displayed indicate the type of automatic gain control being used by the Receiver. If both the words MAN and either SHORT, MEDIUM or LONG are present under the word AGC in the display, the Receiver is being operated in an automatic gain control mode with a manually set threshold.

d. MODE
AM
CW
USB
I-USB
I-LSB
FM
AUX

Located in the middle of the Mode/Meter LCD, the word MODE is always present. The words AM, CW, USB, LSB, I-USB, I-LSB and FM indicate the detection mode of the Receiver. The word AUX is an operator initiated forced bandwidth set-up which is discussed in greater detail in SECTION V, Maintenance, of this instruction manual.

NOTE

The I-USB and I-LSB functions can only be activated if the ISB option (A5) is installed.

e. TUNING
FAST
SLOW
LOCK
BFO
REMOTE

Located in the lower right corner of the Mode/Meter LCD, the word TUNING is always present. The words FAST and SLOW, when displayed, indicate the rate of frequency change per revolution of the manual tuning knob (refer to Paragraph 3.2.8). The word LOCK, when displayed, indicates that the manual tuning knob is disabled. When the words FAST, SLOW and LOCK are not displayed, the Receiver is in the "fine" tuning mode.

If the word BFO is present on the display, the manual tuning knob may be used to vary the BFO frequency but will not change the main receiver LO frequency. The word REMOTE is displayed under two conditions: (1) control of the Receiver is under a remote device the (A6A1 circuit assembly) and (2) the Receiver is executing a BITE test routine whether under LOCAL control or initiated remotely.

3.2.10 Right (Frequency Data) Liquid Crystal Display (LCD)

a. FREQUENCY MHz

Indicates the tuned frequency, in MHz, of the Receiver. Additionally, during a BITE test sequence routine, a two-digit numerical error code will be displayed if BITE encounters any failed test. (Refer to SECTION V, Maintenance.)

b. BFO/LEVEL

Indicates selected BFO frequency in kHz with plus (+) or minus (-) sign to indicate direction of offset from IF frequency. When in the CW mode and BFO CENTER is activated, the display shows a single zero (0). When RF DIG pushbutton key-switch is pressed and held, this area of the display will indicate a relative signal level of the tuned signal frequency from 0-150 or three dashes if this level is exceeded. When depressing the THLD pushbutton key-switch, the BFO data is replaced by the desired signal threshold for the indicated frequency, as set by the operator, and stored for stop-on-signal conditions in either the sweep or scan modes.

c. CHANNEL

The channel number display, when illuminated, indicates that the data displayed is from the indicated channel.

3.2.11 FAULT Indicator (LED)

A red Light Emitting Diode (LED) indicator lamp will be illuminated if there is a failure in the first, second or BFO frequency synthesizers.

3.2.12 SCAN Indicator (LED)

When in the Delta Mode (Delta indicator on), the green SCAN LED indicates that this channel has been selected for inclusion in the cell scan. When in the Receiver Mode (Delta indicator off) the green SCAN LED indicates that the Receiver is operating in the Scan or Sweep mode. The indicator will also flash if the sweep or scan function is halted due to a signal threshold decision.

3.2.13 Delta (Δ) Indicator (LED)

An amber LED is used to indicate the Delta (Δ) Mode. In the Delta Mode, front panel parameter changes may be made and displayed without effecting current Receiver operation or settings.

3.3 OPERATING INSTRUCTIONS

The RA6793A HF Receiver is internally controlled by a microcomputer which measures and controls many more functions than previously available Receivers. Actual control of the Receiver's parameters is performed by control software contained in Eraseable Programmable Read-Only Memory (EPROMs) within the Receiver. Additionally, a self-diagnostic feature (inclusion of Built-In-Test-Equipment, BITE) allows the Receiver to perform self-test upon command for both local (operator) and remote (computer) control, and report back status data through the addition of data communications capability. While this may increase internal circuit complexity somewhat, actual operating procedures become more simplified.

Additionally, the operator is able to further test the Receiver after BITE has finished its analysis by depressing the appropriate pushbutton switches and observing selected Liquid Crystal Displays (LCDs) on the Receiver front panel. The operator can also verify proper operation by performing system connections checks, tuning to local AM broadcasts, observing the signal strength meter, and monitoring the audio from the receiver.

Before attempting to operate the receiver, it is recommended that: (1) verification of systems connections installation be made in accordance with the procedures detailed in SECTION II of this manual; (2) the System Interface checks have been performed as presented in Paragraphs 3.3.1 and 3.3.2 of this section; and (3) a thorough review of the front-panel controls and indicators described in Paragraphs 3.1 through 3.2.13 of this section has been accomplished.

3.3.1 RA6793A Receiver Options Installation Check

The purpose of the Options Installation Check is to verify proper Receiver operation after options have been installed, and before the Receiver has been physically installed in its operating location. The check is divided into three parts:

a. IF Bandwidth Filter Installation Check
b. Remote Interface Check
c. ISB Option Check

Perform the check(s) appropriate to the configuration of the Receiver being tested. Prior to performing these checks, ensure that:

(1) The Receiver is connected to a suitable power source, and that the pc wafer and fuse match the available line voltage in accordance with SECTION II, Paragraph 2.3.4.1.

(2) The Receiver is energized (accomplished by switching the POWER ON switch to the ON position; observing that edgelighting is present; and observing that some data is displayed in the MODE and FREQUENCY LCD's).

NOTE

If the Receiver fails to energize, check the power source, fuse, and/or SECTION V of this manual.

(3) The Reciever is in the LOCAL operating condition, which is accomplished by observing the MODE LCD to determine if the word REMOTE is present. If the word REMOTE is not present in the display, proceed with the desired checks. If it is present, momentarily depress and then release the LOCAL/REMOTE pushbutton switch. This should remove the word REMOTE from the display and place the Receiver in the LOCAL operating condition.

NOTE

If unable to establish the LOCAL operating condition refer to SECTION V of this manual.

3.3.1.1 Optional IF Bandwidth Filter Installation Check

This check is used to verify that the proper IF Bandwidth (plug-in type) filters have been installed in the Receiver, and that the filters are functioning properly. To perform the check:

a. Ensure that the preliminary steps listed in Paragraph 3.3.1 have been performed.
b. Ensure that the IF Bandwidth Filters have been installed in accordance with SECTION II, Paragraph 2.3.3.1.
c. Note the numbers displayed in the Frequency LCD and write them down.
d. Depress and hold the LOCK pushbutton switch.
e. While depressing the LOCK pushbutton, depress the AM pushbutton switch.
f. Release both pushbuttons.
g. Observe the FREQUENCY MHz LCD. Digits in the display should be rapidly changing, and should continue to change for approximately one minute. If, during this period, the display should stop changing and display a two-digit number, there is a problem with either the filters or with the Receiver itself. Should this condition exist, refer to SECTION V of this manual. If the numbers stop changing after the one-minute period and return to the numbers noted in step c, the IF Bandwidth Filters are installed correctly.
h. Momentarily depress and then release the AM pushbutton switch. The word AM should be displayed under the word MODE in the Mode LCD.

i. Momentarily depress and then release the BW pushbutton switch. Note the number displayed to the left of the word BW kHz in the upper right center of the MODE LCD. This number should approximately mate ±25% the bandwidth value of the narrowest filter installed. (NOTE: LSB or USB filters expected, if installed.) The LSB and USB filters can be recognized by the part number stamped on the top of the filter as follows:
LSB filter, 2700 Hz: part number 08409.
USB filter, 2700 Hz: part number 08410.

j. Repeat step i for pushbutton switch. The displayed value for the BW should approximate the bandwidth value of the second narrowest filter then the third; etc.

k. If, in steps i and j, the bandwidths displayed nearly match or slightly exceed the bandwidth values of the installed filters, the filters are functioning properly. If one or more filters do not match or slightly exceed the displayed values, replace the filter(s) in question in accordance with SECTION II, Paragraph 2.3.3.1, and repeat steps i and j until the values do match.

l. Record the value of the filter installed in each slot for future reference. This completes the IF Bandwidth Filter Installation Check.

3.3.1.2 Remote Interface Check (Serial Asynchronous Interface)

The purpose of the Remote Interface Check is to verify the proper operation of the A6A1 assembly. To perform this check:

a. Ensure that the preliminary procedures outline in Paragraph 3.3.1 have been performed.

b. Connect a suitable remote controller, with its connector wired in accordance with SECTION II, Paragraph 2.3.4.6, to the A6A1W1J1 connector on the receiver rear panel.

c. Energize the remote controller and "ask" the Receiver to send its operating parameters to the controller for display. Refer to Paragraph 3.3.4 Remote Control Operation. The ASCII command string for this request is:

$99GCR

where:

$99 addresses receiver number 99 (use the number required for addressing the receiver undergoing test),

G is a "GET" command asking for operating parameters,

CR is "Carriage Return".

d. Note the remote controller display. If any operating parameter information has been displayed at all, the remote interface is working properly. If no data is returned or displayed, refer to SECTION V of this manual and replace the A6A1 module if required. This completes the Remote Interface Check.

3.3.1.3 ISB Option Check

The purpose of the ISB Option Check is to verify the proper operation of the A5 ISB and the ISB/SSB link on the A4 Main IF module. To perform the ISB Option Check:

a. Ensure that the preliminary procedures outlined in Paragraph 3.3.1 have been performed.
b. Refer to SECTION II, Paragraph 2.3.3.3 step 2 and set the I-LSB line level. If the line level can be set, the IF portion of the A5 modules and the ISB/SSB link are functioning properly. If the line level cannot be set (no signal indication or low signal indication), replace the A5 module. (Refer to SECTION II, Paragraph 2.3.3.2 for installation procedures.)
c. Connect a headset to the PHONES jack on the Receiver front panel and adjust the AF GAIN potentiometer until a signal is heard. If a signal can be heard, the audio portion of the A5 module is operating properly. If no signal is heard, replace the A5 module.
d. If both steps b and c produce satisfactory results, the A5 ISB option is fully operational. This completes the ISB Option Check.

3.3.2 RA6793A Receiver/System Interface Check

The purpose of this check is to verify proper operation of the receiving system once the Receiver is installed in its operating location. Prior to performing this check, ensure that the Receiver Options Installation Check(s) outlined in Paragraph 3.3.1 have been completed. To perform the Receiver/System Interface Check:

a. Physically install the Receiver in its operation location.
b. Connect the system RF signal source (antenna; output from multicoupler, etc.) to the RF IN jack J1 on the receiver rear panel.
c. Connect the system audio line to the AF OUT connector J3 on the receiver rear panel.
d. Connect the system external reference frequency source (if used) to REF IN/OUT connector J7 on the receiver rear panel and set the IN/EXT REF switch S2 to EXT.

NOTE

If the Receiver's internal reference is to be used, connector J7 is not used and S2 is set to INT.

e. If the Receiver IF is to be sampled for system use, connect the sampling cable to IF connector J2 on the rear panel. If ISB IF is to be sampled, connect a sampling cable to ISB IF OUT J9 connector on the rear panel.
f. Connect a suitable ground wire to the GROUND terminal on the receiver rear panel.
g. Connect a headset to the PHONES jack on the receiver front panel.
h. Connect the Receiver to a suitable power source by connecting the power line cord to the A10J1 assembly on the receiver rear panel.

CAUTION

Ensure that the voltage value printed on the visible portion of the pc wafer in the A10J1 assembly matches the available line voltage as outlined in SECTION II, Paragraph 2.3.4.1. Failure to match the Receiver to the available line voltage may result in blown fuses or failure of the Receiver to activate.

i. Energize the Receiver by switching the POWER ON switch on the receiver front panel to the ON position.
j. Initialize the Receiver. (Refer to Paragraph 3.3.3.1 for initialization procedures.) The Receiver will initialize itself in approximately one minute. If after initialization, only a two digit number is displayed in the frequency LCD, and the word REMOTE remains in the Mode LCD, refer to SECTION V of this manual.
k. Energize (as required) the remaining equipment in the system.
l. Tune the Receiver to a known signal such as a local AM radio station (refer to Paragraph 3.3.3.1 for tuning procedures) and optimize reception so that the signal is clear and intelligible in the headset or speaker. If no signal is heard, try a different signal. If the signal still cannot be heard, check the antenna, multicoupler (if used), antenna cables, RF IN connector, etc. If still no signal is heard, refer to SECTION V of this manual.
m. Verify that the AF output from the Receiver is present and is being processed by the system AF analysis equipment.
n. Verify that the IF output (if used) is present and is being processed by the system IF sampling equipment.

NOTE

If either the IF (if used) or AF signals are not present at the input to the analysis equipment, check the appropriate cables and/or connectors. (Especially verify the wiring of mating connector for J3 AF OUT on the receiver rear panel.)

Once satisfactory results have been obtained in steps i through n, the Receiver System Interface Check is complete and the system is operational.

3.3.3 LOCAL Control Selection

There are two possible control conditions for operation of the RA6793 HF Receiver. In the first or LOCAL control condition, the receiver functions are controlled by selecting modes, levels, bandwidths, etc., using controls physically mounted on the Receiver itself. In the second or REMOTE control condition, the functions are selected by using a coded message sent by a remote operating terminal. It should be noted that when the Receiver is placed in the REMOTE condition, the controls on the Receiver itself are non-functional. Determination of which condition the Receiver is in (i.e. LOCAL or REMOTE) can be made simply by checking the lower-right corner of the receiver's mode LCD. If the Receiver is in REMOTE, the word REMOTE will be displayed. If the Receiver is in LOCAL, no word will be displayed. Switching between the two conditions is achieved by pressing and releasing the LOCAL/REMOTE pushbutton switch if the unit has an RS-232 Asynchronous Interface, if an IEEE Interface or any special IO is fitted this will not be the case.

3.3.3.1 LOCAL Control Operation Checklist

The following procedures are to be used to operate the RA6793A HF Receiver in the LOCAL control condition:

a. Turn POWER ON switch to ON position. Indications that the Receiver is energized include:

(1) Edgelights illuminated.
(2) Some data shown in Liquid Crystal Displays (LCD's).
(3) Sounds in audio device (headphones or speaker). If Receiver does not energize when POWER switch is toggled, refer to SECTION V of this manual.

b. Establish LOCAL control. Momentarily depress the LOCAL/REMOTE pushbutton switch while observing the lower-right corner of the mode LCD. Depress the switch again. Note that the display will show the word REMOTE on alternate pressings of the switch, while REMOTE disappears on alternate pressings. When the Receiver is under LOCAL control, the word REMOTE is not shown in the display.

c. Initialize the Receiver. The RA6793A Receiver has a built-in capability to self-determine the values of the IF bandwidth filters installed. These bandwidths assignments normally, except when low frequency option installed, use forced bandwidth setup. (The remainder of the initialization process is a series of Built-In Test Equipment (BITE) checks which are addressed in SECTION V.)

To initialize the Receiver:

(1) Press and hold the LOCK pushbutton switch.
(2) While holding down the LOCK pushbutton, press the AM pushbutton switch.
(3) Release both the LOCK and AM pushbuttons simultaneously. The normal indications that the Receiver is in the initialization process are:

(a) The word REMOTE will appear in the Mode LCD.
(b) The frequency LCD will begin displaying a series of rapidly changing digits in both the FREQUENCY and BFO portions of the display.
(c) Rapidly changing sounds and tones in the audio device (speaker or headset.)
(d) Changing modes and levels in the Mode LCD.

Indication that the initialization process is complete is obtained by observing the word REMOTE in the Mode LCD. When REMOTE is erased and the Receiver returns to the displayed values that were present prior to the initialization process, the process is complete. (NOTE: The initialization process takes approximately one minute to complete.) If during the process the display stops changing and a two-digit number appears and remains in the FRQUENCY LCD, BITE has detected a problem in the Receiver. Refer to SECTION V of this manual.

d. Selected Desired Frequency (00.500000 MHz to 29.999999 MHz). There are two methods for selecting any desired frequency. The first of these is to enter the frequency directly using the ENTER pushbutton switch and the numeral pushbutton switches. The second is to select a tune rate and manually tune to the desired frequency using the manual tuning knob. The procedures for each of these methods are as follows:

(1) Direct Entry:

(a) Momentarily depress and release the ENTER pushbutton switch.

(b) Starting with the lefthand digit of the desired frequency, momentarily depress then release the corresponding numeral pushbutton switch.

NOTE

Frequencies less than 10.0000 MHz require an initial zero (0) digit entry. The decimal point will automatically appear in the display without a decimal point entry from the operator.

EXAMPLE 1:
Desired Frequency: 14.2514 MHz
Keystrokes Required:

ENTER
1
4
2
5
1
4
0
0

Resulting Display in FREQUENCY LCD: 14.251400
EXAMPLE 2:
Desired Frequency: 3.75 MHz
Keystrokes Required:

ENTER
0
3
7
5
0
0
0
0

Resulting Display in FREQUENCY LCD: 03.750000
EXAMPLE 3:
Desired Frequency: 0.57 MHz
Keystrokes Required:

ENTER
0
0
5
7
0
0
0
0

Resulting Display in FREQUENCY LCD: 00.570000.

(2) Manual Tuning:
Ensure that the word LOCK is not present in the mode LCD. IF it is present, momentarily depress then release the TUNE RATE pushbutton switch. The word LOCK should disappear. If LOCK cannot be removed from the display, refer to SECTION V of this manual.

e. Select Tune Rate. This is accomplished by alternate depressions of the TUNE RATE pushbutton switch. Observe the right side of the Mode LCD. One of three displays should be present under the word TUNING: SLOW, FAST, or no display (refer to Paragraph 3.2.9). These three displays correspond to three rates of change of frequency caused by rotation of the Manual Tuning Knob as follows:

No display: Fine 1 Hz tuning,
SLOW: Slow 30 Hz tuning,
FAST: Fast 100 Hz tuning.

Rotate Manual Tuning Knob to desired frequency changing tune rates as desired.

EXAMPLE:
Receiver is set at 20.179000 MHz, and the desired frequency is 10.853000 MHz.

(1) Select FAST tune rate.
(2) Tune to approximately 10.8 MHz, using Manual Tuning Knob.
(3) Select SLOW tune rate.
(4) Tune to approximately 10.85 MHz using Manual Tuning Knob.
(5) Select fine tuning rate.
(6) Tune to 10.853000 MHz using Manual Tuning Knob.

f. Select Detection Mode (AM, CW, USB, LSB, ISB U/L, FM). Detection modes are selected by momentarily depressing and then releasing the appropriate pushbutton switch. A discussion of operation in each mode follows.

g. AM.

(1) Depress and release the AM pushbutton switch. Indications that the Receiver is in the AM mode are: the word AM under MODE in the Mode LCD; (b) a one or two digit number next to BW KHZ in the upper right corner of the Mode LCD.

If unable to achieve these indications, refer to SECTION V of this manual.

(2) Select desired IF bandwidth using BW pushbutton. To select a bandwidth, depress and release the bandwidth selection pushbutton BW from one to five times to correspond with BW1 through BW5. The bandwidth of the filter selected will appear next to the BW KHZ words in the mode LCD.

NOTE

If no-number bandwidth appears, re-initialize the Receiver. If the condition persists, refer to Section V of this manual.

(3) Select Gain Control (AGC, MAN, SHORT, MED, LONG). There are three choices for IF Gain Control:

(a) Automatic (AGC)
(b) Manual
(c) Automatic with Manual Threshold.

A discussion of these choices follows.

h. Automatic (AGC). AGC automatically establishes and maintains a desirable IF signal level. Through the use of operator selectable response times, it also establishes the time it takes for the AGC circuitry to respond to IF signal level changes. To select AGC:

(1) Observe the mode LCD under the word AGC. If the word MAN is displayed, momentarily press and release the MAN pushbutton switch. The word MAN should disappear. In addition, another word (LONG, MED, or SHORT) should be displayed under AGC on the display.

(2) Select the response time by depressing and releasing the desired pushbutton switch (LONG, MED, or SHORT). The receiver is now under automatic gain control.

i. Manual. Manual gain control allows the operator to set a desired IF signal level, and disables the automatic response and adjustments to changes in IF signal level. To select manual gain control:

(1) If the word MAN is not present under the word AGC on the Mode LCD, momentarily depress and release the MAN pushbutton switch. The word MAN will appear on the display.
(2) If under the word MAN another word (LONG, MED, or SHORT) is present, momentarily depress and release the pushbutton switch which corresponds to the displayed word. Once the word MAN is the only displayed word under AGC on the mode LCD, the receiver is under manual gain control.
(3) Observe the level meter display in the upper left corner of the Mode LCD. If the word RF is displayed proceed to (4). If the word AF is displayed, momentarily depress and release the METER RF/AF pushbutton switch to change the display to RF.
(4) Once RF is displayed in the mode LCD and the Receiver is under manual gain control, the IF GAIN potentiometer may be adjusted to the desired signal level by rotating the knob while observing the RF level indication on the meter in the mode LCD.

j. AGC with Manual Threshold. This gain control capability allows the operator to manually set the desired IF signal level which the AGC automatically maintains. Response times are operator selectable through the LONG, MED or SHORT pushbutton switches on the lefthand keypad. To select AGC with manual threshold:

(1) Select manual IF gain control as directed in (j).
(2) Set desired signal level as desired according to j.(4).
(3) Momentarily depress and release the desired response time pushbutton switch (LONG, MED, or SHORT).

The Receiver is now under AGC with manual threshold control. Indications that the Receiver is in this condition are:

(a) The word MAN is displayed under the word AGC in the mode LCD, and

(b) The word LONG, MED, or SHORT is displayed under the word MAN in the mode LCD.

k. CW. Select the CW mode by depressing and releasing the CW pushbutton switch. Indications that the Receiver is in the CW mode are:

(a) The word CW under MODE in the mode LCD, and
(b) The appearance of digits under BFO KHZ on the FREQUENCY LCD.

Select BFO (Beat Frequency Oscillator) Frequency (-8.0, 0, +8.0 kHz). The BFO may be operated in either of two conditions:

(a) BFO - adjustable
(b) BFO CENTER - non-adjustable.

NOTE

BFO functions can be controlled by the operator only in the CW mode, and is disconnected from control in all other modes.

l. The BFO condition allows the operator to tune the BFO manually to achieve the desired audio frequency for received CW signals. The BFO CENTER condition allows the operator to zero-beat (fine tune the Receiver to the exact RF) the incoming CW signal. To select BFO Frequency (adjustable):

(1) Observe the BFO KHZ portion of the FREQUENCY LCD. If a three digit number and a "+" or "-" sign is displayed proceed to step (2). If a single zero preceeded by a "+" or "-" sign.
(2) Observe the mode LCD and note the display under the word TUNING. If the word BFO is displayed under tuning, or if SLOW, FAST, or LOCK is displayed, momentarily press and then release the BFO pushbutton switch. The word BFO should now be be displayed under the word TUNING on the mode LCD.
(3) Rotate the manual tuning knob while observing the BFO KHZ portion of the FREQUENCY LCD. The numbers displayed should change as the knob is rotated.
(4) Select the desired BFO Frequency (+8.0 kHz to -8.0 kHz) either by watching the BFO KHZ display while rotating the knob until the desired BFO Frequency is attained, or by listening to the audio signal while rotating the knob until the desired audio frequency is heard.

m. To select BFO CENTER (for zero-beating the incoming signal):

(1) Observe the BFO KHZ portion of the frequency LCD. If a single zero preceeded by a "+" sign is displayed, proceed to step (2). If a three digit number preceeded by a "+" sign is displayed, momentarily press and then release the BFO CENTER pushbutton switch. A single zero preceeded by a "+" sign should now be displayed.
(2) Observe the mode LCD and look under the word TUNING. If there is no word displayed under TUNING or if SLOW or FAST are displayed, proceed to step (3). If either the word LOCK or the word BFO is displayed, momentarily depress and then release the TUNE RATE pushbutton switch. The word LOCK or BFO should disappear.
(3) The incoming signal may now be fine-tuned by slowly rotating the manual tuning knob until the audio tone from the signal is nulled.

(4) Momentarily depress and then release the BFO CENTER pushbutton switch and observe that a three digit number preceeded by a "+" or "-" sign appears in the BFO KHZ portion of the FREQUENCY LCD.
(5) Momentarily depress and then release the BFO pushbutton switch. The word BFO should appear in the mode LCD.
(6) Slowly rotate the manual tuning knob until the desired BFO Frequency is obtained.
(7) Momentarily depress and then release the LOCK pushbutton switch. This disables both the manual tuning and BFO adjustment functions preventing loss of the signal if the manual tuning knob is inadvertently rotated.
(8) Select IF bandwidth as outlined in h. (2).
(9) Select gain control as oultined in h. (3).

n. USB or LSB

(1) Select either upper sideband or lower sideband mode by momentarily depressing and then releasing the appropriate (USB or LSB) pushbutton switch. Either USB or LSB should appear under the word MODE on the mode LCD.
(2) All other functions in USB or LSB are identical to the AM mode (except for IF bandwidth, which is fixed in either the USB or LSB mode).

o. ISB U/L (available only if ISB option A5 assembly is installed)

(1) Select the independent sideband mode by momentarily depressing and then releasing the ISB U/L pushbutton switch on the lefthand keypad. The word I-USB or I-LSB should appear under the word MODE on the mode LCD. Subsequent depressing and releasing of the ISB U/L pushbutton will alternately display I-USB and I-LSB.

NOTE

If the ISB option is <u>not</u> installed, depressing the ISB U/L pushbutton switch will have no effect on Receiver operation.

(2) Other functions are identical to those of the AM mode.

NOTE

Each sideband is independently controlled in this mode. Therefore separate AGC settings are possible for both I-USB and I-LSB.

p. FM.

(1) Select the FM mode by momentarily depressing and then releasing the FM pushbutton switch on the lefthand keypad. The word FM will appear under the word MODE in the mode LCD.
(2) Other functions are identical to those of the AM mode.

q. Forced IF Bandpass Filter Bandwidth Setup. In case BITE results are unsatisfactory, or if the receiver requires initialization when using low frequency options, the forced IF bandpass filter bandwidth setup can be

initialized by simultaneously depressing the LOCK and ISB U/L pushbutton switches, and observing the AUX indicator displayed in the MODE LCD. This process accesses RAM within the microprocessor circuit card assembly (A6A2) for loading of the IF bandpass filter bandwidth complement. It should be noted, however, that this setup cannot be accomplished during the BITE routine. In addition, the setup can be terminated (if desired) before all seven filter slots FL1-FL7 have been changed, and when all seven filter slots have been loaded, the AUX indicator will go off (disappear) erasing any current changes and resetting the receiver to its previous condition.

(1) Symmetrical Filter Entry

NOTE

Entry of symmetrical filters is accomplished using the 0-9 numeral pushbutton switches, in 100 Hz steps, delimited with the ENTER pushbutton switch. For example, to enter a .4 kHz (400 Hz) filter, the "4" and "ENTER" pushbutton switches would be depressed; to enter 20 kHz, the "2", "0", "0", "ENTER" pushbutton switches would be depressed (200 x 100 Hz = 20 kHz).

(a) Depress and release the appropriate numeral pushbutton switches (0-9) on the right-hand keypad, then depress and release ENTER pushbutton switch.

NOTE

In the case of blank filter slots, load by depressing the ENTER pushbutton switch only.

(2) USB and LSB Filter Entry

(a) Depress and release USB and/or LSB pushbutton switch(s) followed by the ENTER pushbutton.

NOTE

In the case of blank filter slots, load by depressing the ENTER pushbutton switch only.

(3) Terminating Forced IF Bandpass Filter Bandwidth Setup:

(a) To abort, depress and release ISB U/L pushbutton switch on the lefthand keypad, and observe AUX indicator displayed go off in the MODE LCD.

(b) Forced IF Bandwidth Setup will terminate automatically following entry of the bandwidth information for the seventh filter.

3.3.4 REMOTE Control Operation

3.3.4.1 Serial Asynchronous Interface. Remote operation with the optional RS-232C remote control interface assembly.

Refer to Appendix A for Input/Output Control messages and status response data tables, and a table of Built-In Test Equipment (BITE) error codes used when accommodating remote control operation. Also a description of the command/monitor data and control functions with the RS-232C.

Before attempting to operate the Receiver in the remote operating condition, it is recommended that the operator be thoroughly familiar with operating the Receiver in the local operating condition (refer to SECTION III, Paragraphs 3.3.3 and 3.3.3.1). "Hands-on" experience working with the Receiver in the local operating condition provides the operator with a working knowledge of receiver capabilities, signal optimization, and control interaction. Such knowledge is essential to obtaining satisfactory results when controlling the Receiver from a remote location.

The minimum considerations when discussing RA6793A HF Receiver remote operation are:

(1) Remote Control Data Character
(2) Remote Control Device
(3) Input/Output Electrical Interface
(4) Remote Control Commands
(5) RA6793A HF Receiver responses to remote control commands
(6) Functions unique to the remote control operating condition.

Each of these considerations is addressed in a following paragraphs.

a. Remote Control Data Character.

The data character used for remote control is the standard ASCII asynchronous format which consists of a start bit, seven data bits (one ASCII Character), a parity bit, and either one stop bit (if a parity bit is used) or two stop bits. Figure 3-2 shows the data character format, and Table 3-1 lists standard ASCII character codes.

b. Remote Control Device

Any remote-control device (terminal, receiver control panel, etc.) which generates and accepts the standard ASCII asynchronous format may be used to control the Receiver.

NOTE

Due to the wide variety of possible control devices, the discussion on remote control commands addresses ASCII characters rather than on specific control pushbuttons, keys, or switches. Similarly, the discussion on RA6793A HF Receiver responses to remote control commands addresses the ASCII characters sent back to the controller, rather than on specific displays generated by the receipt of those responses.

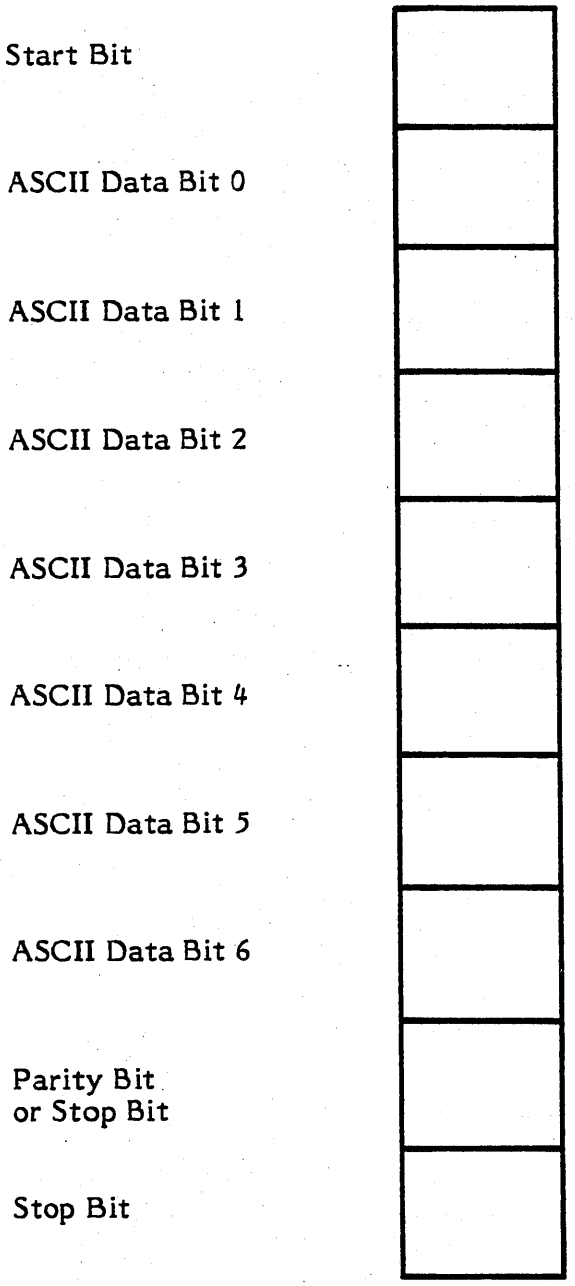


Figure 3-2. Data Character Format

Table 3-1. ASCII Character Codes

ASCII CHARACTER	OCTAL CODE	DECIMAL CODE	ASCII CHARACTER	OCTAL CODE	DECIMAL CODE
NUL	00	0	SP	40	32
SOH	01	1	!	41	33
STX	02	2	'	42	34
ETX	03	3	#	43	35
ETO	04	4	$	44	36
ENQ	05	5	%	45	37
ACK	06	6	&	46	38
BEL	07	7	'	47	39
BS	10	8	(	50	40
HT	11	9	)	51	41
LF	12	10	*	52	42
VT	13	11	+	53	43
FF	14	12	,	54	44
CR	15	13	-	55	45
SO	16	14	.	56	46
SI	17	15	/	57	47
DLE	20	16	Ø	60	48
DC1	21	17	1	61	49
DC2	22	18	2	62	50
DC3	23	19	3	63	51
DC4	24	20	4	64	52
NAK	25	21	5	65	53
SYN	26	22	6	66	54
ETB	27	23	7	67	55
CAN	30	24	8	70	56
EM	31	25	9	71	57
SUB	32	26	:	72	58
ESC	33	27	;	73	59
FS	34	28	<	74	60
GS	35	29	=	75	61
RS	36	30	>	76	62
US	37	31	?	77	63

Table 3-1. ASCII Character Codes

ASCII. CHARACTER	OCTAL CODE	DECIMAL CODE	ASCII CHARACTER	OCTAL CODE	DECIMAL CODE
@	100	64	(Apost)	140	96
A	101	65	a	141	97
B	102	66	b	142	98
C	103	67	c	143	99
D	104	68	d	144	100
E	105	68	e	145	101
F	106	69	f	146	102
G	107	70	g	147	103
H	110	71	h	150	104
I	111	72	i	151	105
J	112	73	j	152	106
K	113	74	k	153	107
L	114	75	l	154	108
M	115	76	m	155	109
N	116	77	n	156	110
O	117	78	o	157	111
P	120	79	p	160	112
Q	121	80	q	161	113
R	122	81	r	162	114
S	123	82	s	163	115
T	124	83	r	164	116
U	125	85	u	165	117
V	126	86	v	166	118
W	127	87	w	167	119
X	130	88	x	170	120
Y	131	89	y	171	121
Z	132	90	z	172	122
[	133	91	{	173	123
/	134	92	:	174	124
]	135	93	}	175	125
	136	94	~	176	126
_	137	95	DEL	177	127

c. Input/Output Electrical Interface.

The input/output electrical interface consists of the A6A1 serial asynchronous interface assembly which connects to the remote control device through the A6A1W1J1 Connector (type M83723-02R-1626N) on the Receiver rear panel. The interface, which provides separate lines for command input and monitor output data, allows up to ten (10) Receivers to be placed on a common, parallel, input/output bus. The command receiver meets the specifications of RS423, RS422 and MIL-STD-188-114, and is also operable with MIL-STD-188C or RS232 compatible remote control devices. The monitor transmitter meets the specifications of RS423 and MIL-STD-188-144, and is operable with MIL-STD-188C or RS232 compatible devices and may be strapped for RS422 unipolar operation. Receiver address baud rate selection, and parity odd/even selection wiring instructions are discussed in SECTION II, Paragraph 2.3.4.6.

d. Remote Control Commands.

If, for example, a Receiver has been designated receiver number 99 and the mating connector for A6A1W1J1 has been wired accordingly, then to remotely control receiver number 99, the following command string (ASCII format) must be sent from the remote control device to the Receiver:

$99S2CR

The "$" character alerts all receivers on the common bus that an address command is coming. "99" alerts Receiver number 99 that all subsequent commands, when they come, will be specifically addressed to it until another "$" character is received. "S2" is a status command which tells the Receiver to set itself to the remote operating condition, and "CR" is carriage return which is the final character sent to the Receiver in each command string. (CR is interpreted by the Receiver as an "execute" instruction, and causes the Receiver to carry out all as an "execute" instruction, and causes the Receiver to carry out all commands in the string; in this case "set up for remote control.")

The other status (S) commands which may be used to follow "$99" are:

S1 Set Receiver to local control
S2 Set Receiver to remote control
S3 Initiate BITE self-test sequence
S4 Terminate BITE selt-test sequence
S5 Report bandwidth of installed IF filter
S6 Report BITE results
S7 Force bandwidth setup (discussed in Section V or 3.3.3.1.q)
S8 Enable remote AGC dump
S9 Inhibit remote AGC dump

Status commands may be sent to only one Receiver at a time since some of the status commands will result in monitor data being sent back to the remote-control device from the Receiver.

Once the Receiver has been set for remote operation by the "S2" command, the next step normally is to initiate the BITE self-test sequence by sending "S3" (quotation marks are used here for clarity only and are not part of the S3

command). The BITE routine requires approximately one minute to complete. After the BITE routine is complete, the "S6" command will cause the Receiver to report its findings. The "S5" command will then report a list of IF filter bandwidths. These bandwidths should be compared with the Receiver configuration chart to determine if the filters are working properly. If the BITE report displays an error code number, refer to SECTION V of this manual. Note that once a particular receiver has been addressed by the "$NS2" command (N is 99 in this case), subsequent commands (S3 or S6 or S5) to the Receiver need not be prefixed by the "$N" (receiver address). A typical command string normally sent to initiate remote control operation is illustrated in Example 1.

EXAMPLE 1:

1st entry: $99S2CR - sets receiver 99 for remote control
2nd entry: S3CR - initiates BITE self-test routine in receiver 99
3rd entry: S6CR - requests BITE routine results from receiver 99
4th entry: S5CR - requests values of IF bandwidth filters found in receiver 99

(Commands "S5" and "S6" will result in data responses from the Receiver to the remote control device.)

5th entry: 57CR - this command is used to force a particular IF bandpass filter bandwidth complement in the receiver. Allowable codes are L for lower sideband (LSB), U for upper sideband (USB), N for none, and bandwidths up to 20 kHz (in kHz) with a resolution of 100 Hz. Symmetrical bandwidths (in kHz) are terminated with a comma. The string may contain all seven IF bandpass filters (FL1-FL7) bandwidths or it may end early with a carriage return (CR). Filter slots not entered will not be altered by the S7 command. A typical command is as follows:

S7LU1.7,.4,N3.2,(LF)

The preceeding command sets up the following:

Filter Slot	Filter/Function
FL1	Lower Sideband (LSB)
FL2	Upper Sideband (USB)
FL3	1.7 kHz (Symmetrical)
FL4	400 Hz (Symmetrical)
FL5	None
FL6	3.2 kHz (Symmetrical)
FL7	Unchanged from previous setting

6th entry: S8CR - this command causes all subsequent commands containing receiver data to cause an automatic AGC dump.

7th entry: S9CR - this command causes the AGC dump to be disabled. This would be used when free tuning the receiver by remote control.

Two additional commands will result in data responses from the Receiver to the remote control device. The commands are called monitor commands and instruct the Receiver to report certain specified data on receipt of the command. The monitor commands are "G" (for "Group") and "T" (for "Talk").

EXAMPLE 2:

The command $99GCR will result in all of the following data (depending on mode) being sent from receiver 99 to the remote control device in the order indicated.

RF Frequency
Detector Mode
Gain Control Mode
IF Bandwidth
BFO Frequency
IF Attenuation
Status

(The actual information sent by the Receiver and its format is shown in the discussion on RA6793A HF Receiver responses to remote control commands.)

"T" commands result in selected data being sent back to the remote control device.

EXAMPLE 3:

The commands $99TFCR will result in only frequency and summary status data being sent to the remote control device.

"T" commands include:

TF - requests frequency data only
TD - requests detector mode data only
TI - requests IF bandwidth data only (non-functional in ISB mode)
TM - requests IF gain control mode data only
TB - requests BFO data only (functional only when Receiver is in BFO variable).
TA - requests IF gain control attenuation data only (functional only when Receiver is under manual IF gain control or AGC with manual threshold.)

Several "T" commands may be sent to the receiver at once by listing the desired information characters after only one "T".

EXAMPLE 4:

$99TFDICR would result in frequency, detector mode, bandwidth and summary status information being sent back to the remote control device. The following commands cause the Receiver to change operating parameters, but do not result in data responses to the remote control device. Therefore, more than one Receiver may be addressed at once by inserting commas (in ASCII format) between the Receiver numbers.

EXAMPLE 5:

The command: $99,14,27,F5CR would result in receiver number 99, 14, and 27 being set to a frequency of 05.000000 MHz.

NOTE

Once multiple receivers have been addressed as in this example, two things must be remembered: (1) any subsequent parameter change command preceding the next $ will result in that parameter being changed on all receivers addressed (in the example, receiver numbers 99, 14, and 27); (2) A status or monitor command may not be sent before the next $, since more than one Receiver cannot respond on the bus at the same time. If a status or monitor command is sent, the command is simply ignored. To change only one receiver's operating parameter(s) or to send a status or monitor command, the desired Receiver must be readdressed individually ($99 or $14 or $27 in Example 5).

Frequency Selection. The command is in the format FN where N is used to select the Receiver(s) operating frequency. The frequency command may specify the desired frequency down to 1 Hz. For example, the command F03.415926 would tune the Receiver(s) to 3.415926 MHz. If an exact frequency is not required, the leading and trailing zeros may be eliminated. The command F3.4 would tune the Receiver(s) to 3.400000 MHz. Note that in both cases a decimal is required to indicate MHz. If an exact multiple of 1 MHz is desired (as in Example 5), "F" followed by the desired MHz number (as in Example 5) may be sent without a decimal point. This will tune the addressed receiver to the exact whole multiple of 1 MHz specified.

Detector Mode Selection. The desired detector mode is selected by sending the command DN where N is the desired detector mode as follows:

D1 - AM
D2 - FM
D3 - CW with variable BFO
D4 - CW with BFO CENTER
D5 - ISB (if ISB option is installed)
D6 - LSB
D7 - USB

BFO Offset. The BFO offset frequency may be set by sending the command BN where N indicates the offset frequency in kHz. For example, the command B+1.82 will set the BFO offset 1.82 kHz above the center frequency; B-4.65 will set the offset 4.65 kHz below the center frequency.

Bandwidth Selection. The desired bandwidth is selected by sending the command IN where N indicates the filter bandwidth in kHz. For example, the command I3.24 would select the 3.24 kHz filter. If a command is received that does not match the filter in the Receiver, the Receiver will automatically select the closest filter. For example, the command I7. will select the 6.8 kHz filter. Note that the decimal point is used to indicate kHz.

Gain Control Mode. The desired gain control mode is selected by sending MN where N is the desired gain control mode as follows:

M1 Selects short AGC time constant
M2 Selects medium AGC time constant
M3 Selects long AGC time constant
M4 Selects manual gain control
M5 Selects short AGC with manually set threshold
M6 Selects medium AGC with manually set threshold
M7 Selects long AGC with manually set threshold

Manually Set Gain Control. The Receiver will respond to remote commands to set a manual gain. The Receiver IF gain is controlled by adding attenuation (from 0 to a maximum of 120 dB) to the amplifier circuit. This feature may also be used in conjunction with the AGC operation to establish a minimum threshold level for the AGC. The command for setting the level is AN where N represents the approximate amount of attenuation (N x 0.8 in dB) to be added to the circuit. For example, the command A3 would add approximately 3 dB of attenuation to the amplifier circuit; A104 would add approximately 80 dB of attenuation.

EXAMPLE 6:

The command $99F2.35D3I1.5M5A55B-1.7CR would result in receiver number 99 to be set to the following parameters:

Selected Receiver: 99
Frequency: 02.350000 MHz
Detector: CW with variable BFO
IF Bandwidth: Closest installed IF bandwidth filter to 1.5 kHz
Gain Control: Short AGC with manually set threshold
Attenuation: Threshold of approximately 40 dB
BFO Frequency: 1.70 kHz below center frequency

e. RA6793A HF Receiver Responses to Remote Control Commands.

Status commands "S5" and "S6", and monitor commands "G" and "T" request data to be sent from the Receiver to the remote control device. This data is obtained and transmitted when the command (followed by a CR) is sent to any one receiver address. The format of the response depends on the data requested.

"S5" triggers a data stream in the following format:

BW(FL1), BW(FL2), BW(FL3), BW(FL4), BW(FL5), BW(FL6), BW(FL7) where BW is the bandwidth in kilohertz and FL1-FL7 is the filter slot checked.

EXAMPLE 7:

The command $99S5CR might obtain the following repsonse:

L,U,1.6,.5,,2.7,16 where
L - Lower sideband filter in filter slot FL1
U - Upper sideband filter in filter slot FL2
1.6 - 1.6 kHz filter in filter slot FL3
.5 - 500 Hz filter in filter slot FL4
,, - No filter in filter slot FL5
2.7 - 2.7 kHz filter in filter slot FL6
16 - 16 kHz filter in filter slot FL7

"S6" triggers a data stream in one of two formats as follows:

:OKNCR, where N is the receiver number and CR is carriage return
or
:X,Y,Z,ENDNCR, where X, Y, and Z would represent the two digit BITE error codes, N is for Receiver Number, and CR is Carriage Return

EXAMPLE 8:

:OK99 indicates that receiver 99 passed all BITE tests
or
:4,17,33END99 indicates that receiver 99 found BITE error codes 4, 17, and 33. (Refer to SECTION V for explanation of BITE error codes.)

"G" triggers a data stream in the following format:

F, D, M, I, B, A, S where:

F is receiver frequency in MHz
D is receiver detector mode
M is receiver gain control mode
I is receiver IF bandwidth
B is BFO frequency (only functional in CW variable BFO mode)
A is IF attenuation (only functional with manual gain control or AGC with manual threshold)
S is receiver status

EXAMPLE 9:

The command $99GCR might result in a response such as F2.35D3M5I1.5B-1.7A55S2 which indicates the following parameters:

Selected Receiver: 99
Frequency: 2.35000 MHz
Detector Mode: CW with variable BFO
Gain Control: Short AGC with manual threshold
IF Bandwidth: 1.5 kHz
BFO Frequency: 1.70 kHz below center frequency
Attenuation: Threshold of 40 dB
Status: Receiver is under remote control

NOTE

Status responses differ from status commands. Refer to next paragraph.

Status Response. The status data is sent as the last item in each monitor response ("G" or "T") from the Receiver. The status data is returned to the remote-control device in the format SN, where N is a one or two digit number representing the following conditions:

0 Receiver is operating in local control operating condition.
1 Receiver is operating in remote control operating condition.
2 Synthesizer is out of lock.

4 Receiver is in the override mode (discussed under Functions Unique to the Remote Control Operating Condition).
8 Last command sequence had character transmission error.
16 Last command sequence had data error.
32 Lost data error in last sequence.

If two or more conditions are present, the numbers representing the conditions will be added together and transmitted as one number. For example, 17 (1 + 16) would indicate that the Receiver is in remote control and last command sequence had a data error; 13 (8 + 4 + 1) would indicate remote control, override mode and character transmission error. Note that some numbers are not valid, i.e. 12 since override mode is impossible while in LOCAL control.

The next status response to be considered to "TX" where X is the desired parameter(s) which triggers a data stream in the following format:

XVS where:

X is the identity letter of the parameter (F, D, M, I, B, or A)
V is the value of the parameter
S is the status response.

EXAMPLE 10:

The command $99TFDCR might obtain a response such as F2.35D3S1 where:

Frequency: 02.350000 MHz
Detector Mode: CW with variable BFO
Status: Receiver is in the remote operating condition.

f. Functions Unique to the Remote Operating Condition

Override Mode. The remote control device may be used to command a Receiver to switch to the override mode. In override mode, some of the automatic operating features of the Receiver are disabled. That is, the first local oscillator is always tuned to 40.455 MHz above the entered RF frequency and IF slot is selected remotely regardless of the type of filter installed. Therefore, the remote controller must decide what the filter should be used for, the type of detection mode to employ, and the BFO offset to receiver a signal.

For instance, in sideband detection with a symmetrical filter, the first local oscillator and BFO must be properly offset to correctly demodulate the signal. The remote controller also assumes the responsibility for ensuring that the filter is installed in the selected slot, since an empty slot will cause a dead Receiver. The override mode blanks the display. In addition, override signals cannot be handed off to the operator, since the machine has no way of deciding the difference between a sideband signal with virtual carrier offset or a CW signal with a BFO offset. The override mode is invoked when both detector and bandwidth are sent in the same command with the = sign. Sending either without the equals stores the = data but removes the Receiver from the override mode and restores it to normal operation. The Receiver will respond to the following override commands (in the format $ND=XI-Y where N is the receiver number, X is the mode selection number, and Y is the filter slot number):

Mode Selection. The desired mode is selected by sending one of the following commands:

D = 1 Selects envelope
D = 2 Selects continuous-wave detector
D = 3 Selects frequency-modulation detector
D = 4 Selects ISB operation.

Note that these "D" commands differ from the normal "D" commands and are unique to the override mode.

Filter Selection. In the override mode the filters are selected according to the filter slot number instead of the filter bandwidth.

The command is I=N where N corresponds to the filter slot number. For example, the command I=3 will select the filter inserted in filter slot FL3.

EXAMPLE 11:

The command $99D=2I=3CR would result in receiver 99 being set to the override mode using the CW detector and the filter installed in the filter slot FL-3.

To exit the override mode, an "IN" command is sent where "N" is the desired bandwidth in kHz (not the filter slot number), and the "=" sign is omitted.

NOTE

When the Receiver is in the override Mode, both the MODE LCD and the FREQUENCY LCD are blanked. In addition, status command S1 will be ignored by the Receiver.

3.3.4.2 Standard Bit-Parallel, Byte-Serial Interface. Remote operation with the IEEE-488C remote control interface assembly.

The RA6793A HF Receiver equipped with the IEEE-488C interface circuit card assembly (A6A1) can function as either a talker, supplying status information to a remote controller, or as a listener, accepting commands from the remote controller. The remote controller selects a particular receiver on the bus through a five bit address, programmed on each receiver at a 5-pole address switch assembly on the rear panel. This address is also used to command the receiver to the talker listener mode.

The remote controller, typically a HPIB calculator computer system or "smart" terminal, equipped with an IEEE-488C interface, can command the receiver to change any operating parameter in the same manner as the front panel controls. Connections between the receiver and the IEEE-488C interface bus are made through a separate rear panel connector (A6A1J2). The data transfer between the bus and the receiver is a standard bit-parallel, byte-serial format. There are 16 primary signal leads between the bus and the receiver. These include: eight data lines (DI01 through DI08), three handshake lines (DAV, NDAC, and NRFD), and five bus management lines, used to specify how the information on the data lines is to be interpreted.

The remote control interface circuit is used primarily as an interface between the bus and the microprocessor circuit card assembly (A6A2) of the receiver. The remote control interface circuit may be divided into three primary circuit groups: the bus driver/receiver circuit, the general purpose interface adaptor circuit, and the microprocessor interrupt circuit. The general purpose interface adaptor, or GPIA, is a large scale integration (LSI) chip that accepts the data from the bus and applies it to the microprocessor. The interrupt circuitry permits the microprocessor to stop its current operation, service and remote controller commands, and then return to its original operation.

Refer to Appendix B for interface requirements and receiver addressing between the RA6793A Receiver and the IEEE-488C bus, and detailed information on command word formatting between the remote controller and the receiver.

3.3.5 Channel Scanning

The RA6793A HF Receiver has a 100 channel memory which may be preset and controlled by the operator. Within this 100 channel memory, random cell scanning may be used to automatically scan any upward sequence of the 100 channels. The dwell time on each selected channel is operator selectable through use of the numerical pushbutton switches.

The following procedures are to be used to operate the Receiver in channel scan:

a. Ensure that the Receiver is under local control and is operating normally in accordance with paragraph 3.3.3.1 Local Control Operation Checklist.
b. Depress the CHAN pushbutton. Note that the Delta indicator becomes illuminated. This indicates that the Receiver has changed from Receiver Mode to Delta Mode.
c. Using the numerical pushbutton switches (0-9), depress two that correspond to the desired channel. Examples: 01, 24, 77, 83, etc. The channel numbers appear in the Frequency LCD.
d. Preset the desired Frequency, Bandwidth, AGC Mode, and/or other parameters using the appropriate front panel controls.
e. Determine whether or not the channel is to be included in the cell scan. If it is to be included, press the SCAN button if necessary to ensure that the SCAN indicator is lit.

NOTE

When the SCAN indicator is lit, which means that the Scan flag is set while the Receiver is in Delta Mode, the Channel being preset will be included in a decade cell scan. If the SCAN indicator is not lit, the channel will be shipped.

f. If it is desired to cause the Receiver to physically change to the data in the displays, press and release the LOAD pushbutton. This will cause the Receiver to tune to the preset. If it is desired to preset the channel without changing the Receiver's current operating conditions, press and release the STORE pushbutton.

NOTE

Using the LOAD pushbutton brings the Receiver back to Receiver Mode (Delta indicator off), while using the STORE pushbutton leaves the Receiver in Delta Mode for presetting additional channels.

g. Preset additional channels as desired using steps b-f of this paragraph ensuring that the scan flags are set for those channels desired to be scanned.
h. Load any channel into the Receiver by pressing CHAN, the two digit channel numbers and LOAD pushbutton. Note that LOAD extinguishes the Delta indicator.
i. Press the SCAN pushbutton. Note that since the Receiver is in Receiver Mode, the SCAN indicator now is illuminated which means that the Receiver is scanning. Observe that the channel number in the Frequency LCD stops momentarily on each channel within the decade whose scan flag is set and that Receiver parameters displayed change to those of the channel being viewed.
j. Set the dwell time (the time the Receiver remains on each channel) by using the numerical pushbutton switches (0-9). "0" selects a dwell time of approximately 100 milliseconds while "9" selects a dwell time of approximately 10 seconds. "2" through "8" select intermediate dwell times of increasing duration respectively.

NOTE

The dwell time may be changed at any time during Scan Mode by pressing another numerical pushbutton.

k. To stop the Scan, press the SCAN pushbutton. To resume the Scan, press SCAN again.

NOTE

Scan may be initiated at any time as long as the Receiver is in the Receiver Mode (Delta indicator off) and there is a channel loaded into the Receiver as indicated by a channel number present in the channel display section of the Frequency LCD.

3.3.6 Shut Down Procedure

Deenergize the Receiver by switching the POWER ON switch on the receiver front panel of the off (down) position.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section describes the general theory of operation of the receiver. A receiver functional block diagram is provided to show signal paths through the receiver. The receiver functional description is followed by individual circuit-level descriptions of each receiver module.

4.2 FUNCTIONAL DESCRIPTION

Figure 4-1 is a functional block diagram of the receiver. This diagram will be used in the following paragraphs to describe the functional signal flow through the receiver. For the purposes of the following descriptions, the receiver is considered to be divided into two major functional sections: RF Processing and Digital Control. These two sections will be described separately.

4.2.1 RF Processing Section

The RF Processing Section consists of five major functional areas: Input Conversion, Local Oscillators, IF Amplification/Demodulation, Audio Switching and AGC.

4.2.1.1 Input Conversion

Antenna signals enter via rear panel RF IN, J1, and are applied directly to the input of Low Pass Filter, A1. The Low Pass Filter is a fixed-tuned, 50 ohm, four-section elliptic filter which band limits the antenna input signals to 30 MHz. A built in protection clamp circuit protects receiver circuitry against RF levels exceeding +27 dBm. The band limited filter output drives the input of 1st Mixer, A2.

The 1st Mixer receives RF input signals from the Low Pass Filter and mixes them with the 1st LO signal from the 1st LO Synthesizer, A7. The first LO signal varies from 40.955000 MHz to 70.454999 MHz, corresponding to receiver tuned frequency settings of 00.500000 MHz to 29.999999 MHz. The 1st Mixer output passes through a bandpass filter to select the 40.455 MHz 1st IF signal and reject all other signals. The 1st IF signal is amplified by a linear buffer which is gain-controlled by the dc gain control voltage derived from AGC circuitry on the Main IF/AF, A4. The 1st IF output from the 1st Mixer, A2, drives the 2nd Mixer, A3.

The 2nd Mixer, A3, receives the 40.455 MHz 1st IF signal from the 1st mixer and initially amplifies it through a 2-stage, narrow band gain-controlled IF amplifier. The amplified 1st IF signal is then mixed with the 2nd LO signal from the 2nd LO/BFO Synthesizer, A8. The 2nd LO signal is fixed at 40.000000 MHz. The 2nd Mixer output passes through a bandpass filter to select the 455 kHz 2nd IF signal and reject all other signals. The 2nd IF signal is amplified by a linear buffer whose output drives the input of the Main IF/AF, A4.

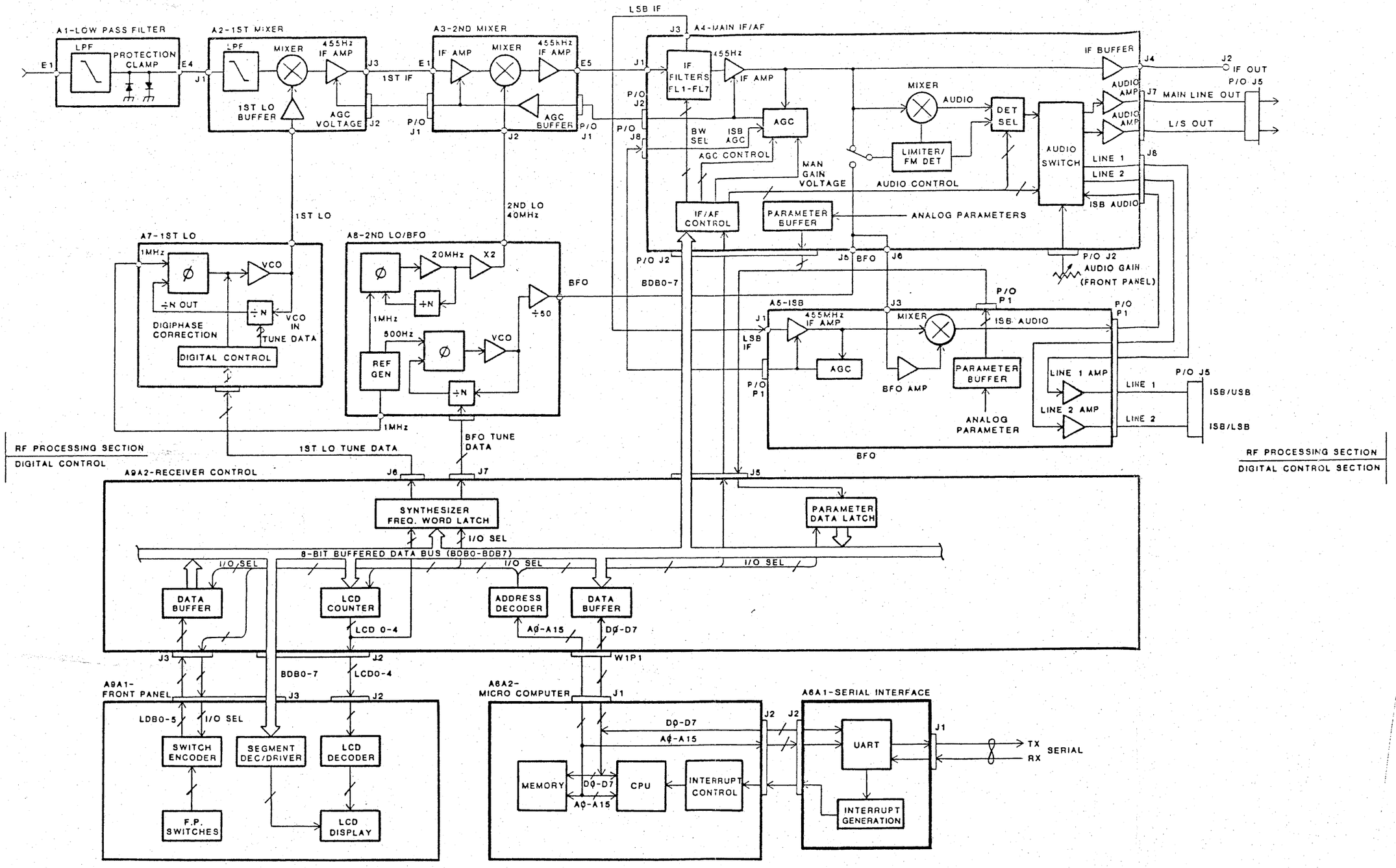


Figure 4-1. Overall Functional Block Diagram

4.2.1.2 Local Oscillators

There are two oscillator synthesizer modules in the receiver: the 1st LO Synthesizer, A7, and the 2nd LO/BFO Synthesizer, A8. These will be explained separately in the following paragraphs.

4.2.1.2.1 1st LO Synthesizer, A7

The 1st LO is programmed with the 1st LO tuning data from the Receiver Control, A9A2. This tuning data drives the 1st LO digital control circuit which decodes the data and sets the divide ratio of the programmable divider. A voltage controlled oscillator generates the basic frequency which drives the programmable divider input. The divider output is compared with an internal 100 kHz by a phase comparator. The comparator output is a dc voltage which drives the voltage controlled oscillator.

When the receiver is set for a tuned frequency of 00.500000 MHz, the digital control sets the programmable divider for an overall divide ratio of 4.0955000. This causes the phase comparator to drive the VCO to an output frequency of 40.955000 MHz. When the receiver is set for a tuned frequency of 29.999999 MHz, the digital control sets the programmable divider for an overall divide ratio of 7.0454999. This causes the phase comparator to drive the VCO to an output frequency of 70.454999 MHz. The digital control also generates a digiphase correction voltage which effectively cancels sidebands on the VCO output caused by the digital averaging process. The VCO output is the 1st LO signal and drives the 1st Mixer LO input.

4.2.1.2.2 2nd LO/BFO Synthesizer

The 2nd LO/BFO Synthesizer consists of an internal reference generator, a 2nd LO fixed loop synthesizer and a variable loop BFO synthesizer. The internal reference frequency is generated by a temperature stable 5 MHz crystal oscillator. This reference signal is used to stabilize the 1st, 2nd and BFO synthesizers.

The 2nd LO synthesizer uses a 20 MHz crystal oscillator as the basic signal generating unit. The 20 MHz signal goes through a fixed divider and is compared with the 5 MHz reference signal by a phase comparator. The phase comparator output is a dc voltage which drives the 20 MHz oscillator. This locks the 20 MHz crystal oscillator to the 5 MHz reference. The 20 MHz oscillator output is then doubled by a frequency doubler to 40 MHz. This is the 2nd LO output which drives the 2nd Mixer LO input.

The BFO is programmed with the BFO tune data from the Receiver Control, A9A2. This tune data directly programs the divide ratio of the BFO programmable divider. A voltage controlled oscillator generates the basic frequency which drives the programmable divider input. The divider output is compared with an internal 500 Hz reference by a phase comparator. The comparator output is a dc voltage which drives the voltage controlled oscillator.

When a BFO offset of -8.0 kHz is commanded, the BFO divider is set for an overall divide ratio of 44700. This causes the phase comparator to drive the VCO to an output frequency of 22.35 MHz. When a BFO offset of +8.0 kHz is commanded, the BFO divider is set for an overall divide ratio of 46300. This causes the phase comparator to drive the VCO to an output frequency of 23.15 MHz. The VCO output is followed by a divide-by-50 divider, yielding an output frequency range of 447 kHz to 463 kHz. This output is the BFO signal and drives the CW/SSB detector on A4 and the ISB detector on A5.

4.2.1.3 IF Amplification/Demodulation

The Main IF/AF, A4, receives the 2nd IF signal from A3 which is coupled directly to seven bandwidth filter slots. The number of filters plugged in and the bandwidth of each filter depends on the option procured. Any number, up to seven, may be plugged into the card at any one time, if optional filters were specified. The filter bandwidth desired for operation is then automatically switched into the IF circuit through a diode switch. This switch is controlled by the buffered data bus from A9A2 through the Main IF/AF control decoder. When the optional independent sideband (ISB) is used, filter slot FL1 must contain a lower sideband filter. This filter may be connected, through a movable link, from the diode switch to a bus that leads directly to the ISB circuit card assembly A5.

The IF signal output of the selected bandwidth filter is impedance coupled to a two stage AGC controlled amplifier. The output of this amplifier is then coupled to a bandpass filter for additional filtering of the IF signal. A portion of this signal is routed through a buffer amplifier to J2-IF OUT, on the rear panel, as the IF output signal.

The IF signal is also coupled through a buffer amplifier to one input of an RF switch and to the product and synchronous AM detector. The RF switch also has the beat frequency oscillator (BFO) as an input with the output of the switch coupled directly to the FM detector. The switch has two modes of operation and is switched through the control circuitry. In the AM and FM modes the switch selects the IF signal; in all other modes, the switch automatically couples the BFO to the FM detector and limiting amplifier. Two outputs of the FM detector are then coupled to a detector select switch and to the carrier input of the product and synchronous detector. The output to the product and synchronous detector will be either the demodulated AM signal or BFO depending on the mode selected. The detector select switch is also controlled by the function modes of the control section. In the FM mode the select switch passes only the FM detected signal to an audio filter. In all other modes the detector select switch passes the output of the product and synchronous detector to the same audio filter.

When the ISB is selected from the control section, the LSB portion of the IF signal is linked directly to circuit card assembly A5. The flow of the IF signal through the ISB circuit is very similar to that just described, except that the BFO is connected directly to the ISB detector. The USB portion of the IF signal is routed through the A4 circuit card in the ISB mode.

4.2.1.4 Audio Switching

The detected audio signal from either the FM detector or the product detector is selected by the detector select switch through the Main IF/AF control decoder. The selected audio is routed through a low pass filter to a crosspoint switch. The control decoder programs the crosspoint switch to select the various audio modes available as outputs from the Receiver. When the ISB option A5 is installed the ISB audio output from the audio amplifiers is also coupled to the switch. In non ISB modes the main audio (A4 card) is selected and routed to two separate audio amplifiers. The first amplifier is volume controlled through the AF GAIN control on the front panel. The output of this amplifier is routed both to the rear panel for loudspeaker output and to the phones jack on the front panel. The second amplifier is level controlled through a variable attenuator placed in the line to the second amplifier by the crosspoint switch. Attenuation is varied through a screwdriver adjustment on the front panel. This amplifier then drives an output transformer which provides the monitor line output to the rear panel. If the ISB circuit card is installed, the non-ISB mode outputs of the attenuator will also be routed through circuits on the ISB card and appear on Line 1 output on the rear panel. This circuit is described in the ISB mode which follows.

In the ISB mode either the main (USB) or the ISB (LSB) is selected and routed to the same circuits as described in non-ISB mode. In addition the crosspoint switch couples both the LSB and USB through variable attenuators to their respective amplifiers on the ISB circuit card. The two amplifiers drive output transformers which couple the USB (Line 1 output) and LSB (Line 2 output) to the rear panel. Level control of Line 1 output is through front panel screwdriver adjustment MAIN LINE LEVEL. Line 2 output is controlled through I-LSB LINE LEVEL. These two adjustments vary the attenuators connected in their respective lines.

4.2.1.5 AGC

The Automatic Gain Control (AGC) provides the Receiver with constant level AF output signal with large variations in the incoming RF signal. The main receiver AGC circuitry is located on circuit card assembly A4. The optional ISB circuit card assembly A5 contains its own AGC for signal gain control in the ISB mode of operation.

The Receiver may be operated in any one of three different gain control modes: manual, automatic, and automatic with a manually set threshold. In the manual mode, the gain is set through a front panel control. In the automatic mode, the AGC circuits will compensate for changes in the receiver input signal level. In the automatic/manual mode, the front panel control is used to set the operating threshold of the AGC circuits.

The AGC operates from a portion of the IF signal taken after the gain control IF amplifier stage, thus maintaining a closed AGC loop. The AGC detects the IF signal, provides three different decay times, and provides for automatic threshold control of the output signal or manual threshold control. The output of the AGC circuit is routed to the second IF amplifier on circuit card assembly A4 by controlling the gain of two IF amplifier stages: one located on circuit card assembly A3 and the other located on circuit card assembly A2.

4.2.2 Digital Control Section

As shown in Figure 4-1, the major elements of the Digital Control are the Microcomputer, A6A2, the Receiver Control, A9A2, the Front Panel, A9A1 and the Serial Interface, A6A1. The Microcomputer directs receiver operations through an 8-bit buffered data bus on A9A2. This bus is the major interface point between the microcomputer, the front panel and the receiver RF Processing Section. The Receiver Control, A9A2, also contains data buffers, latches and I/O Select generators necessary to permit communication between the buffered data bus and the rest of the receiver.

4.2.2.1 Microcomputer Operation

The Microcomputer, A6A2, consists of a CPU, ROM/RAM memory and the Interrupt Control. Reset circuitry generates a reset signal when power is applied. This forces the CPU to initialize all circuitry to its starting condition and causes the ADDRESS to move to the starting address of the control ROM program.

The microcomputer directs all operations and communicates with other receiver control circuits through its 8-bit bidirectional data bus. Temporary storage for receiver settings and for data computation is provided by the working RAM. The CPU reads data into and out of the RAM via the data and address busses. The system operating program is contained in ROM. The CPU reads data out of the ROM via the data and address busses.

The CPU, under program control, receives data from the front panel switches, sends data to the front panel displays and sends data to the RF processing section via the buffered data bus on A9A2. This bus interfaces with the microcomputer data bus through a data buffer. Selection of the various front panel and receiver RF circuits is performed by the CPU address bus through an address decoder on A9A2.

The basic functions performed by microcomputer (A6A2) include:

a. Initialize circuits following power-up to establish microcomputer interfacing and control over the Digital Control Section.

b. Read local input signals from panel switches.

c. Update front panel displays.

d. Compute and send tuning data to receiver local oscillators.

e. Compute and send operating data to the main receiver IF/AF.

f. Read parameter status data from the main receiver IF/AF.

g. Receiver commands from the remote controller.

h. Perform a Built In Test (BIT) for the receiver.

4.2.2.2 Front Panel Switches

As shown in Figure 4-1, the front panel switches connect to the buffered data bus through data buffers. These switches are continually read, in program sequence, by the CPU. The switches are selectively addressed by the I/O decoder data, LDB0-5, and is read onto the buffered data bus through a data buffer. The read data is then transferred to the CPU data bus for storage in RAM.

4.2.2.3 Front Panel Display

The tuning mode and frequency indicating displays are continuously updated by the CPU. Display data is transferred from the buffered data bus to the LCD display through the segment latch/drivers. Display data drivers drive all displays in common. Individual displays are enabled for display through the LCD 0-4 bus generated by the Secondary Address Counter. The secondary address counter coordinates with display data on the buffered data bus to transfer the correct display data to the desired display latch/drivers chip.

4.2.2.4 Oscillator Tuning Data

Tuning data to the 1st LO and the BFO is generated, under program control, by the Synthesizer Frequency Word Latch. The 1st LO data consists of a strobed and clocked serial data stream. The transfer of the 1st LO data is coordinated by the I/O decoder output which controls data being transferred to the 1st LO displays. BFO data consists of a BCD word representing actual desired BFO frequency.

4.2.2.5 Receiver Operating Data

Main IF/AF operating data is transferred directly to A4 from the buffered data bus. This data is used to control BW, AGC and audio output routing. Control of this data within A4 is coordinated by the I/O Select bus from A9A2.

4.2.2.6 Parameter Status Monitoring

Analog parameter data from A4 and A5 is transferred directly to the buffered data bus through parameter buffers and a parameter data latch. This data is continually read, in program sequence, by the CPU. The I/O Select Bus, under program control, selectively transfers the parameter data to the buffered data bus through the data latch. The data is then transferred to the CPU data bus for storage in RAM.

4.2.2.7 Remote Control

The CPU receives and sends data to the remote controller via the Serial Interface, A6A1. The serial interface communicates with the CPU via the CPU data and address busses. A UART in A6A1 interfaces the CPU data bus to the serial data stream connecting to the remote controller. The UART sends an interrupt request to the CPU whenever the remote controller sends data or commands. This forces the CPU to halt its normal program sequence and service the remote controller commands and data.

4.2.2.8 Built In Test Equipment (BITE) Functional Overview

The BITE system of the Receiver performs two major functions. First, it determines, organizes and displays the bandwidth of the IF filters installed in the Receiver. This allows the installation of these filters in any slot, with minimum limitations. Second, BITE performs tests of functionality of the receiver modules. These tests provide overall verification of the operation of the receiver, and specific verification of the operation of selected modules. BITE performs the following functional tests in the Receiver: Readability of the RAM in the microcomputer; lock condition and timing of all phase locked loops; settling time in the frequency synthesizers; operation of the IF AGC; operation of the ISB AGC detector if it is installed; and measuring the bandwidth of all of the IF filters. In order for the receiver to pass the above tests, all modules must have been operating properly. However, the A1, A4, A5 and A6A1 modules are not interrogated.

To initiate BITE from the front panel, the operator must press both the LOCK and the AM pushbuttons simultaneously, then release. The CPU then executes the BITE sequence. Test results are displayed as a two-digit error code on the front panel display. BITE is terminated at any point by depressing LOCK and LSB simultaneously, then releasing. The following is a brief discussion of each of the BITE tests:

a. CPU - All bytes of RAM are tested proper read and write capabilities.

b. 2nd LO/BFO - Lock status of the 2nd LO is verified. BFO is stepped from -8.0 kHz to +8.0 kHz in 500 Hz steps and lock is verified at each step.

c. 1st LO - 1st LO is stepped from 0-30 MHz in 0.5 MHz steps. Stepping time and lock is verified at each step.

d. IF/AF - Test signal is injected. CW detector and BFO are enabled. AGC voltage is verified. Audio output is verified. Manual gain operation is verified.

e. ISB - Test signal is injected. BFO is enabled. AGC voltage is verified. Audio output is verified.

f. IF Filters - FL1 is checked for symmetrical or unsymmetrical filter present. If ISB is installed, FL1 must LSB. FL2-FL7 are checked for presence or absence of filters. Slots containing filters are checked for bandwidth by sweeping the 1st LO and monitoring IF output level.

Specific instruction for utilizing the BITE routine and interpreting the error code results are provided in paragraph 5.2.4.

4.2.3 POWER SUPPLY

Refer to Figure 7-16, Main Chassis Assembly Schematic Diagram, as an aid in understanding the following description. The power supply provides the various dc voltages required throughout the Receiver. The unit, located on assembly A10, contains a step-down transformer, diode rectifiers, filter capactiors, regulators and an alternate 1/2 amp 250V fuse. Primary input power is controlled through a POWER ON switch located on the front panel. This primary input power may be either 100, 120, 220 or 240 volts from 43 to 420 Hz. The proper voltage is selected through a pc wafer and voltage selector located on the rear panel of the Receiver. The step-down transformer provides three different voltages for rectification, filtering and regulation. Six different dc voltages are provided at the output of the power supply. These voltages are +20 Vdc regulated, +15 Vdc regulated, +15 Vdc unregulated, -15 Vdc regulated, +5 Vdc regulated and +5 Vdc unregulated.

4.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs provide a detailed circuit-level description of each of the Receiver modules. Descriptions are provided in numerical, rather than functional, order. Simplified block diagrams are used throughout the text to simplify the description. These block diagrams should be used in conjunction with the schematic diagrams in Section VI.

4.3.1 Low Pass Filter, A1

Refer to Figure 7-1, RF Low Pass Filter Schematic Diagram, as an aid in understanding the following description. The incoming RF signal is passed from the RF IN connector J1 through terminal E1 to the lightning arrestor circuit. The lightning arrestor consists of spark-gap E3, static drain resistor R1 and series current protection fuse F1. This circuit protects the receiver from high voltage impulse-type discharges. The RF signal is then passed to an 8-pole elliptic lowpass filter. The nominal impedance of the filter is 50 ohms and insertion loss is less than 3 dB from 0 to 30 MHz. Above 35 MHz, the attenuation increases rapidly. This attenuation eliminates interference caused by image frequencies from 81.4 to 111.4 MHz or by IF feedthrough at 40.455 MHz, and prevents local oscillator reradiation. Zener diodes CR1-CR4 from a bipolar clamping circuit which protects the receiver from damage by sustained RF levels in excess of +27 dBm.

4.3.2 First Mixer, A2

Refer to Figure 4-2, First Mixer Functional Block Diagram, as an aid in understanding the following description. It consists of a signal lowpass filter, first mixer, bandpass filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the first local oscillator frequency of 40.955 to 70.455 MHz.

4.3.2.1 RF Signal Lowpass Filter and Mixer

The output of the A1 module is connected to the first mixer through a two section elliptical lowpass filter (L15-C23, L11-C24-C25 and L12-C26-C27), which has a cut off frequency of 35 MHz and serves to present a 50 ohm termination to the mixer, U1, RF input port. This filter operates much in the same manner as the RF input filter. It offers a very low loss to the incoming wanted RF signal, but an increasingly high loss to frequencies

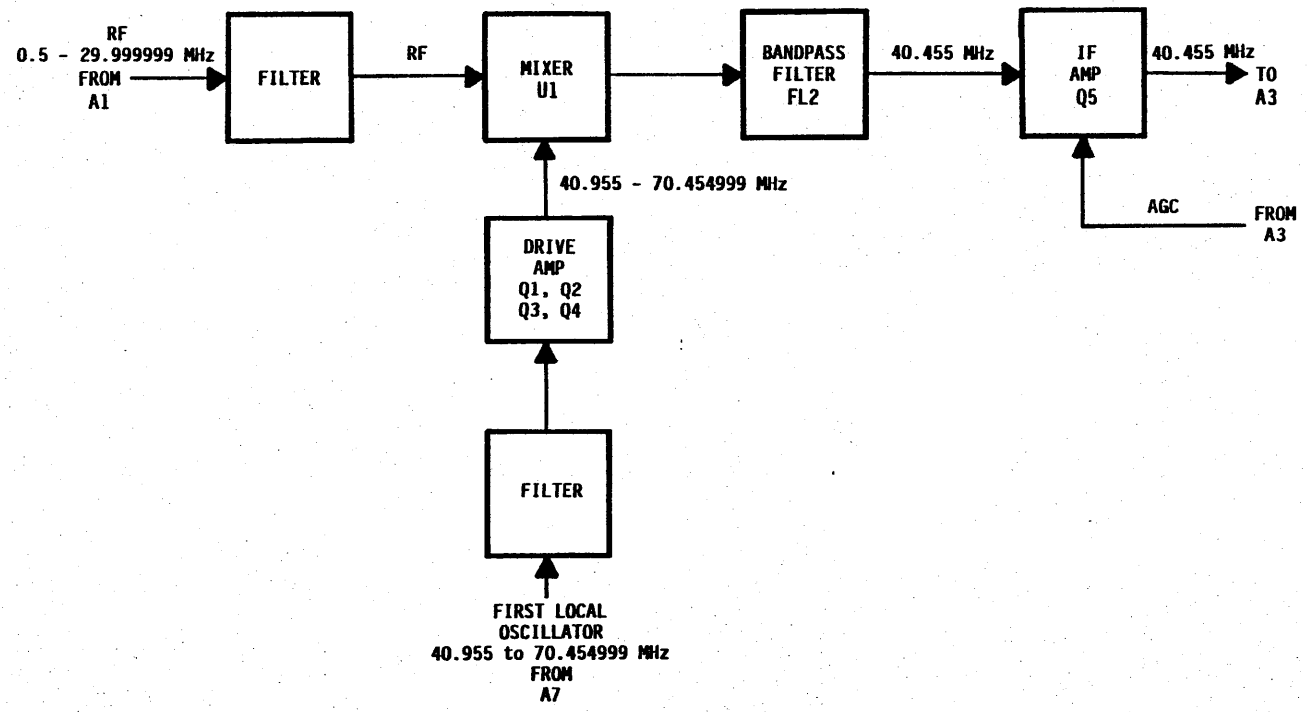


Figure 4-2. First Mixer Functional Block Diagram

above 30 MHz. The mixer, U1, is used for mixing both the incoming RF signal (0.5 to 29.999 MHz) and the first local oscillator signal (40.955 to 70.455 MHz). The resultant frequencies are taken from the mixer, and filtered to provide a difference frequency of 40.455 MHz to form the first IF signal.

4.3.2.2 First Local Oscillator Input Filter and Drive Amplifier

The filter for the incoming first local oscillator signal is an 8-pole elliptic high pass filter exhibiting high attenuation for undesired signals below 40 MHz. The output of this filter is coupled to a common emitter amplifier Q2 through capacitor C9 and resistor R3. The mixer drive amplifier is comprised of transistors Q1, Q2, Q3 and Q4. The local oscillator signal from the filter, which may be monitored at TP2, is coupled to the base of common emitter amplifier, Q2, whose current is regulated by transistor Q1. The voltage at the base of Q1 is set by divider R1 and R2 which in turn sets the potential at the emitter of Q1. Thus the current through R6 is regulated by bias control of Q2 via R6 and L6. The output of Q2 is capacitance-coupled (C21 and C22) to a complementary pair amplifier made up of PNP transistor Q3 and NPN transistor Q4. The output of this pair is applied directly to transformer T1 to drive the LO input to mixer U1. The mixer also receives the RF input from A1 as described above.

4.3.2.3 AGC Controlled IF Amplifier

The output of the mixer is coupled to a bandpass filter FL1. This crystal bandpass filter is designed to reject all the resultant mixer frequencies, except the difference frequency of 40.455 MHz with a bandwidth of 20 kHz. This bandwidth provides an additional option in the AM, FM, or CW modes of operation. This first IF signal is coupled through C47 to an impedance matching network of L19, C53 and R21, and to a linear amplifier consisting of field effect transistor Q5. A dual tapped transformer, T3, makes up part of the load circuit of Q5, to which is connected a current controlled AGC signal. This AGC signal, in effect, varies the impedance of the load transformer which in turn varies the gain of Q5. A second signal from the AGC circuit is applied to the gate of Q5 which varies its bias in relation to the AGC signal strength. This results in a high linear AGC controlled first IF signal, for ouptut to the the second mixer circuit card assembly A3.

4.3.3 Second Mixer, A3

Refer to Figure 4-3 Second Mixer Functional Block Diagram, as an aid in understanding the following description. It consists of a three stage AGC controlled first IF amplifier, a bandpass filter, a mixer and output second IF amplifier. Input signals to the circuit card include: the first IF signal from A2, AGC signal from A4, and the second local oscillator signal from A8. The output signals consist of AGC output to A2 and the second IF signal to A4. Figure 7-3 shows the schematic diagram for the second mixer, A3.

4.3.3.1 First IF Amplifier

The first IF amplifier consists of three stages with the second stage gain controlled from the AGC signal. The third stage drives the signal for input to the bandpass filter. The 40.455 MHz signal routed from A2 is coupled to the drain of field effect transistor Q1, through capacitor C1. The grounded gate of this stage provides high gain for input to filter FL1 through capacitor C5. Filter FL1 provides for rejection of all frequencies other than the 40.455 IF signal. The output of the filter is connected through capacitor C6 to the drain of field effect transistor Q2, which also has a grounded gate. The load circuit of Q2 consists of resistors R16 and R18 and a dual tapped transformer T1. The AGC signal is connected to one tap of the transformer and in effect, varies the impedance of the load transformer. This action varies the gain of the amplifier in relation to the AGC signal. The output of this stage is taken from the second tap on the transformer and coupled to the base of NPN

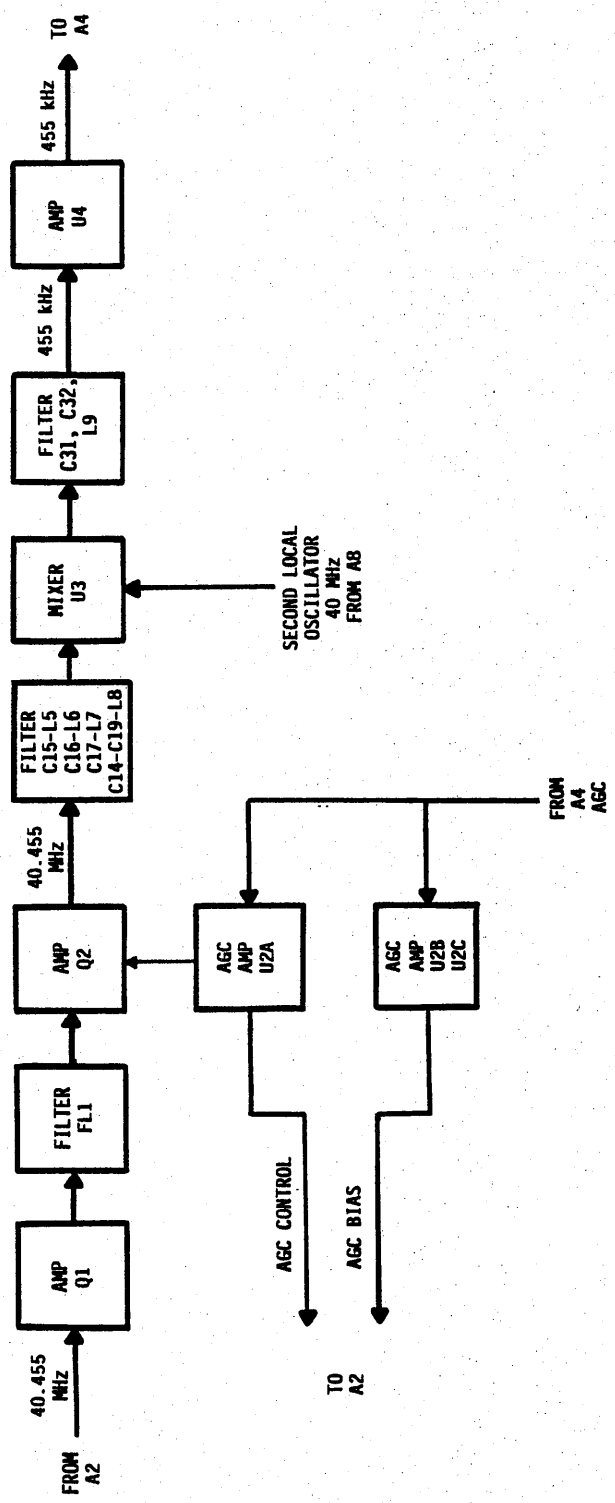


Figure 4-3. Second Mixer Functional Block Diagram

transistor Q3, through capacitor C11 and resistor R20. A variable coil that forms part of the first section of a four section bandpass filter is connected into the load circuit of Q3. The output of the Q3 is, therefore reflected directly into the bandpass filter. A variable resistor R26 in the emitter circuit of Q3 provides for gain adjustment of this stage.

4.3.3.2 Bandpass Filter, Mixer and Second IF Amplifier

The bandpass filter consists of four tunable tank circuits (C15-L5, C16-L6, C17-L7, and C14-C19-L8). Each stage is tuned to resonate at the first IF signal frequency. The output of this filter is coupled directly to the input of integrated circuit mixer U3. A 40 MHz signal from the second local oscillator is connected to a second input of the same mixer. The difference frequency is the second IF signal, 455 kHz. All other frequencies are rejected through the filter consisting of capacitors C31 and C32 and coil L9. The output of the mixer, U3, is connected to a tapped load transformer T2. The output is taken from that transformer tap and coupled through C24 and the filter, just described, to an integrated amplifier U4. This stage provides amplification for the second IF signal output from A3.

4.3.3.3 AGC Amplifier

A two section AGC amplifier is contained on circuit card assembly A3 which provides for both voltage and current control of a signal from AGC circuit on A4. This controlled AGC signal is applied to two IF signal stages for level control. One of the IF stages controlled is located on circuit card assembly A2 and described in Paragraph 4.3.2.3. The second AGC controlled IF amplifier is on A3 and is described in Paragraph 4.3.3.1. An AGC signal from the AGC circuit on A4 is routed through resistor R2 to two separate amplifiers. The first amplifier is a two stage feedback amplifier consisting of integrated operational amplifiers U2B and U2C. The highly regulated output of this amplifier is routed to circuit card assembly A2 and used as the bias control to the gate of that output IF amplifier. The same AGC signal through resistor R2 is routed to an integrated operational amplifier U2A. This amplifier has both its negative and positive inputs regulated through voltage regulating transistor U1A (positive) and U1B (negative). The action of these transistors control the bias voltage to the operational amplifier which in turn controls its output current flow. The output of this amplifier stage is then coupled to transistor U1C which amplifies the signal and applies it to the IF amplifier through resistor R19 and diode CR1. The diode prevents IF signal feedback to the amplifier. This signal then controls the gain of that IF amplifier in relation to the AGC signal from A4. The output of the operational amplifier U2A is also coupled to the base of transistor U1D which buffers the signal for application to the IF amplifier stage on A2.

4.3.4 Main IF/AF, A4

The Main IF/AF circuit card assembly A4 contains IF circuits, AF circuits, and AGC circuits. The description of these circuits are divided into those three basic functions and shown in three separate simplified block diagrams in Figures 4-4, 4-5, and 4-6. Receiver control circuits are also contained on A4 and are described under the A9 circuit card. Input signals to the circuit card include: the second IF signal from A3, the BFO signal from A8, audio and AGC signals from A5 and control signals from A9. Output signals from the board include: second IF signal to A5, BFO, audio and AGC signals to A5, audio signals to A9 and to the rear panel, AGC signals to A3, and control signals to A9.

4.3.4.1 IF Circuits

Figure 4-4 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4. This circuitry consists of the bandpass filters, their switching circuitry, a four stage IF amplifier, an IF output amplifier, an RF switch, a limiting

amplifier and FM detector, and a product a synchronous AM detector. The second IF signal routed from A3 is connected directly to seven 455 kHz bandpass filter sockets FL1-FL7. These sockets provide for plugging in up to seven optional preselected filters of various bandwidths. These filters optionally available in bandwidths from 0.4 kHz to 16 kHz, may be changed at the customer's discretion. Selection of a particular installed filter is then accomplished automatically through the receiver control system. Each filter socket is connected to a diode switch which is controlled from the receiver control circuits. The output of the diode switch for filter FL1 must be linked to the common output of all the other filter switches, if it is used in A4 operation. If it is to be used for the ISB operation, then it must be linked to the output for that circuit card, assembly A5. The receiver control is programmed to select and switch into the circuit the filters in ascending order of bandwidths, regardless of the order in which they are plugged into the sockets; that is, when BW1 is selected, from receiver control, the narrowest bandwidth contained in the seven sockets (six if ISB is installed) will automatically be selected. BW2 will select the next widest bandwidth and so on with BW5 selecting the widest bandwidth. Two filters are generally reserved for USB and LSB operation, which are also selected automatically when those modes of operation are called for through receiver control.

The common output of the diode switch which consists of CR1 through CR14, R9 through R22 and C21 through C27, is connected through resistor R25 to the base of transistor Q1. This emitter follower stage acts as a buffer between the diode switch and the input to a two stage IF amplifier U8 with AGC control. An incoming AGC signal is applied to each stage of the integrated circuit amplifier and provides for level control of the IF signal. A variable resistor R39 connected between the output of the first stage and the input of the second stage provides for manual adjustment of the gain of the IF signal. Variable resistor R47 is used for adjusting the AGC signal level. The output of the two stage IF amplifier is connected to a filter consisting of capacitors C44, C46 and C47, resistor R50 and tunable coils L1 and L2. This double tank circuit provides for rejecting unwanted spurious signals. The output of the filter is routed through capacitor C49 to two separate functions: a three stage IF output amplifier and an emitter follower amplifier Q6. the first stage, Q7, of the IF amplifier is an emitter follower which provides buffering between the incoming signal and the second stage Q8. This second stage amplifies the signal and connects it to still another emitter follower stage Q9 for buffering to the IF OUT connector J2, located on the rear panel.

The emitter follower amplifier A6 acts as a buffer in the same manner as Q7 above but its output is routed to three separate functions: the AGC detector circuit, the product detector and the FM detector through the RF switch. The signal routed to the AGC detector is described under AGC control circuits. The IF signal routed to the FM detector U18 through the RF switch CR22-CR25 is operated by Receiver control. Receiver control directs the switch to connect the IF signal to the detector in the AM and FM modes only. In all other modes of operation, the RF switch connects the BFO signal to the FM detector U18. The IF signal routed to the product detector is connected to its signal port. All signals applied to the FM detector: AM, FM or BFO are connected to a limiting amplifier which removes modulation from the AM carrier and passes it or BFO through the output carrier of the FM detector to the carrier input of the product detector. In the FM mode the signal is detected, its carrier rejected, and an audio signal, from the detector audio output, is connected to the detector select switch. This switch, an integrated circuit transistor gate U19A will select the detected FM audio, only in the FM mode, as directed by receiver control. In all modes except FM, a carrier frequency (AM or BFO) is applied to the carrier input of the product detector. In all modes of operation the signal selected, through receiver control, appears on the signal input of the detector. The detector removes the carrier and routes the audio, through its output, to the detector select switch U19A described above. Receiver control directs this switch to select that audio in all modes except FM.

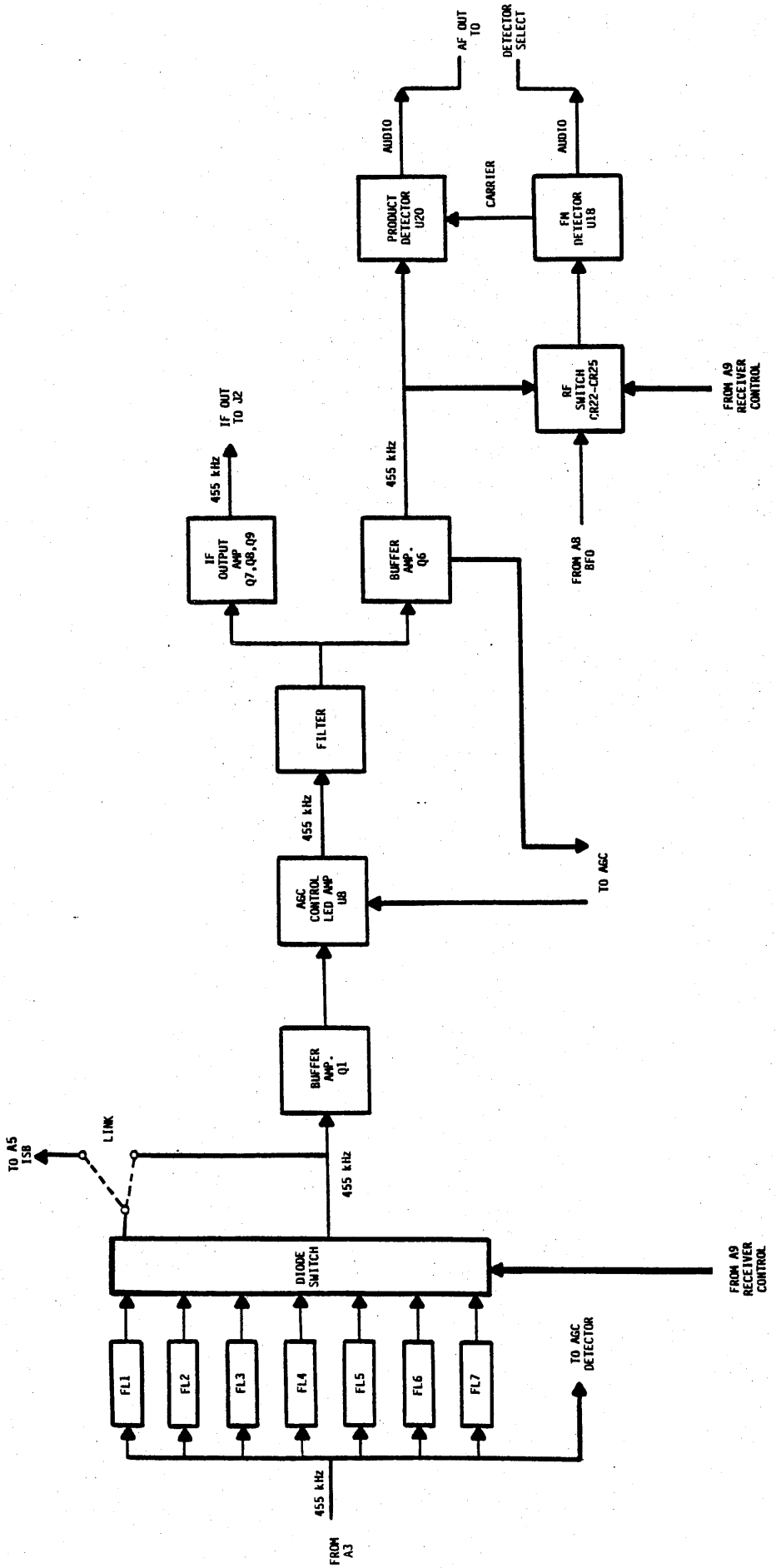


Figure 4-4. A4 IF Circuits Functional Block Diagram

4.3.4.2 AF Circuits

Figure 4-5 shows a functional block diagram of the audio circuits contained on circuit card assembly A4. This circuit consists of an audio lowpass filter stage, a crosspoint switch, two attenuators and two output amplifiers. The audio signal from detector select, U19A, is connected through capacitor C85 to a lowpass filter and amplifier U28. The filter rejects any unwanted frequencies above the audio frequency that might have passed through the detector. The amplifier U28 operates in two different modes. In the AM and FM modes transistor switch U19B disconnects capacitor C113 from the circuit while in all other modes the capacitor is connected across R128, effectively shunting this resistor, thus reducing the signal level in these modes. The output of amplifier U28 is connected to an audio crosspoint switch U25. This switch, through Receiver control, controls audio switching from A4 circuits described above and from the optional A5 circuit card when installed. In non-ISB modes the switch routes the A4 signal to the AF GAIN input and to variable attenuator U30. The signal through the AF GAIN control is coupled through capacitor C96 to an audio output amplifier U26. The output of this amplifier is coupled through C108 to AF OUT connector J3 on the rear panel and to the PHONES jack on the front panel. The signal, through variable attenuator U30, is routed to connector J8 for output to the ISB circuit card and is also routed back to the crosspoint switch. The switch, in this non-ISB mode, connects the attenuated signal through capacitor C95 to a second audio output amplifier on integrated circuit U26. This amplifier drives transformer T1 through C107 and is coupled to the Monitor Line output on connector J3 on the rear panel. The variable attenuator is controlled through screwdriver adjust MAIN-LINE LEVEL located on the front panel and provides level control of the main (A4) audio signal to the Monitor Line output in the non-ISB mode.

In the ISB mode either main (USB) or ISB (LSB) is selected and routed to the same circuits described in non-ISB mode. In addition, the crosspoint switch couples both the USB and LSB through variable attenuators to their respective amplifiers on the ISB circuit card. The USB is routed through attenuator U30 and controls the signal as described in non-ISB mode. The LSB signal is routed through attenuator U31 to J8 and back to the crosspoint switch in the same manner as USB. Attenuator U31 is controlled through screwdriver adjust I-LSB LINE LEVEL located on the front panel and provides level control of the LSB (A5) audio signal. The LSB and USB are routed through connector J8 to their respective amplifiers on circuit card A5 and returns through circuit card A4 to Line 1 Output (USB) and Line 2 output (LSB) on AF OUT connector J3 on the rear panel.

Two audio signals are routed to the AF metering circuit contained on circuit card A4. One signal is tapped from the AF GAIN control input and the second signal from the monitor output amplifier. These two signals are connected to transistor gate U19C which selects between the two signals on direction from Receiver control. In all modes except BITE the signal from the monitor output amplifier is selected and routed to the AF metering circuit. This circuit is described under AGC circuits.

4.3.4.3 AGC Control Circuits

Figure 4-6 illustrates a functional block diagram of the AGC circuitry contained on circuit card assembly A4. The circuits consist of an AGC detector, AGC decay, peak signal detector, decay time constants, an integrator, filter, a gain control distribution amplifier, a digital-to-analog converter and various electronic switches controlled from receiver control circuits. The description also includes the AF/RF meter comparator circuit.

The AGC circuitry is designed to provide three modes or techniques for controlling the gain of the Receiver: manual, automatic and automatic with a selectable threshold. In the automatic mode the level of the IF amplifier U8 is controlled automatically with three

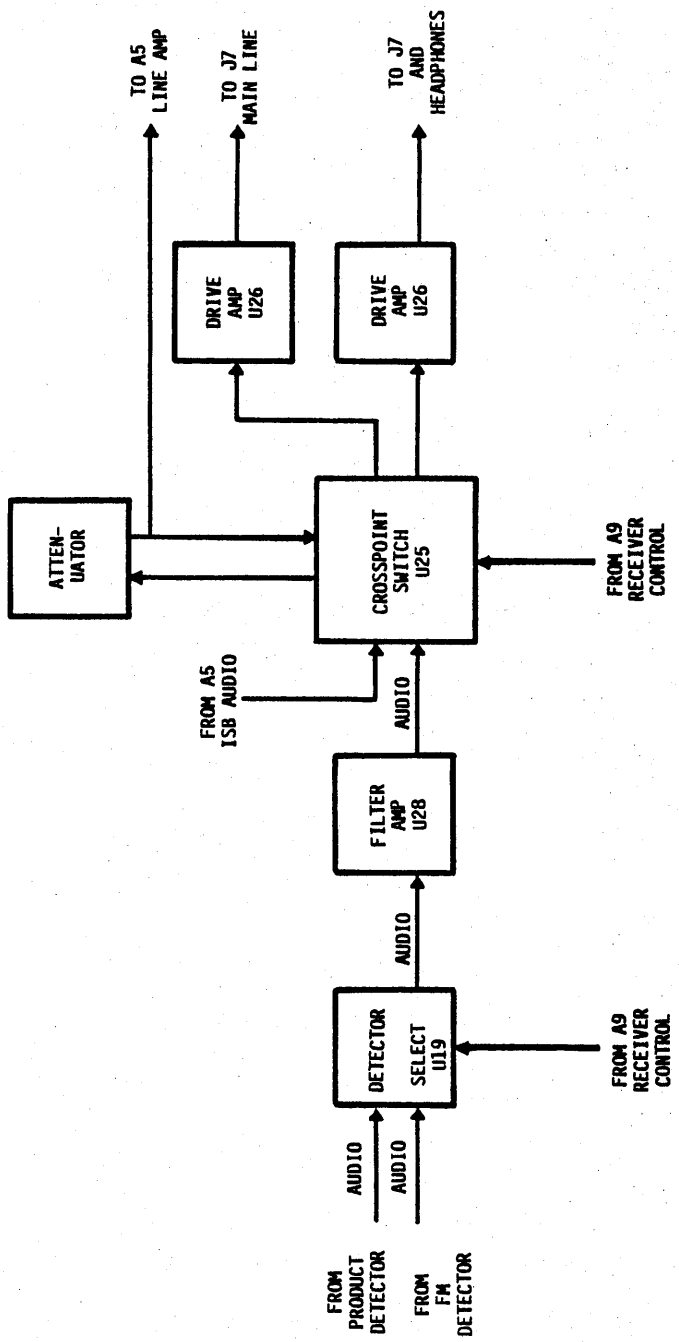


Figure 4-5. A4 AF Circuits Functional Block Diagram

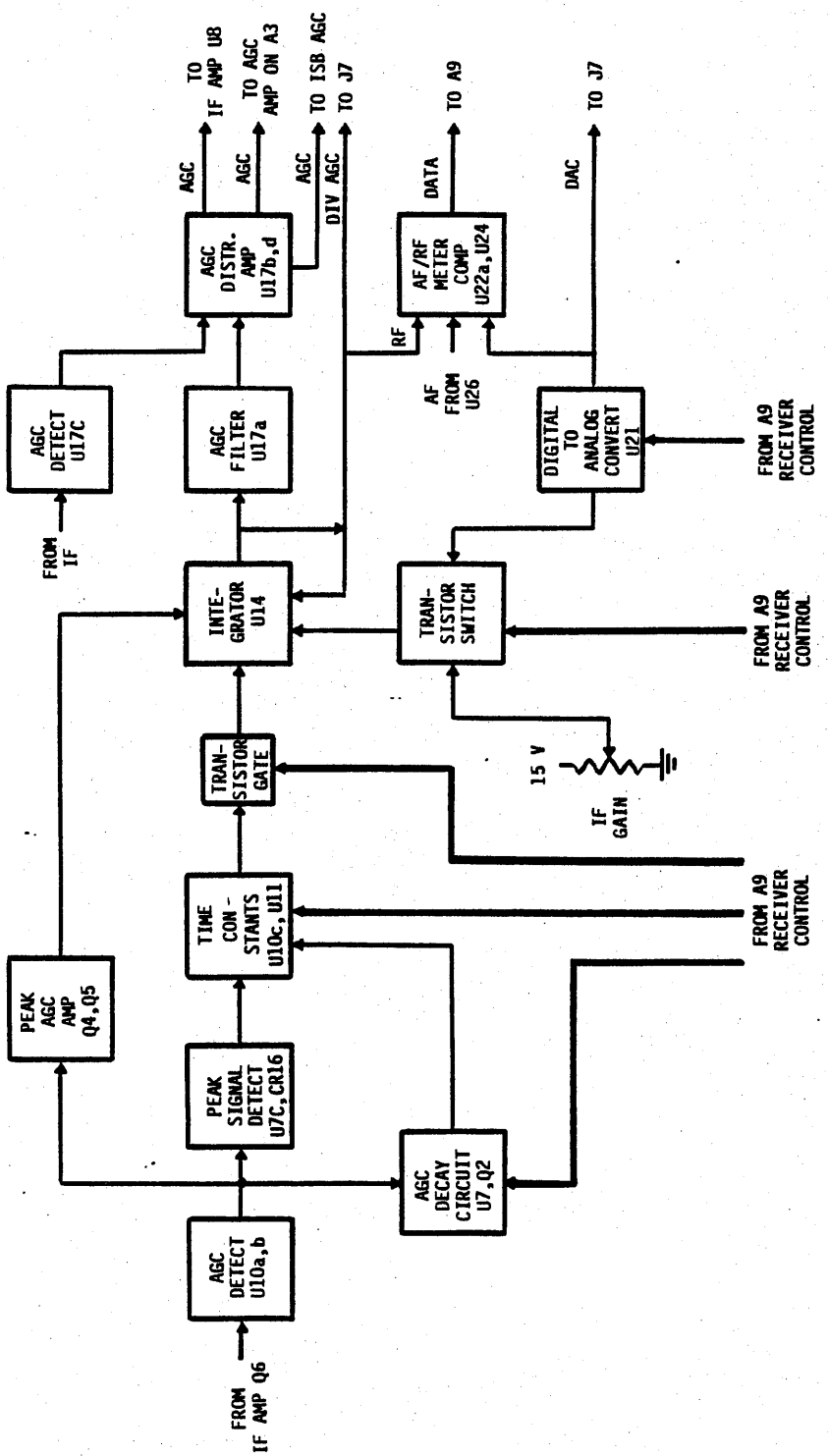


Figure 4-6. A4 AGC Circuits Functional Block Diagram

selectable decay times; SHORT, MEDIUM and LONG. In the manual mode the IF GAIN control is used to control the level of the AGC signal applied to the IF amplifier U8. The IF GAIN control is used to select the threshold in the automatic with selectable threshold mode. The same decay times as in automatic are selectable in this mode.

An IF signal taken from IF emitter follower Q6 is coupled through capacitor C31 to U19A for detection. The three transistor array U10 acts as a detector to the IF signal with U10C connected as an emitter for buffering the DC signal to two circuits: AGC decay and peak signal amplifier. Peak signal amplifier U7C couples the signal, across a decay time select circuit, to integrate amplifier U14A. The signal routed to the hang circuit which consists of amplifier U7A and U7B is time controlled through capacitor C42, resistors R45 and R146 and transistors Q2 and Q10. When short time decay is selected, Receiver control turns on transistor Q2 and transistor gate U12A. Capacitor C42 is shorted to ground through transistor Q2 which turns on transistor U10D and a short delay is asserted using combination resistors R52 and R55. When medium time decay is selected transistor Q10 and transistor gate U11A is asserted. Capacitor C42 discharges through the parallel resistance of R45 and R146, providing a short hang time, after which U10 is turned on and a medium delay is asserted through R52 and R53. When long time decay is selected, capacitor C42 discharges through R45, providing a long hang time, after which U10 is turned on with decay time asserted through R52.

The AGC applied to integrator amplifier U14A is mixed with signals from diversity AGC through amplifier U14B and gain control or threshold from amplifier U14C when AGC mode dictates. In the manual mode both transistor gates U11C and U12B are enabled through receiver control and the gain control voltage is asserted directly to the input of R14A. In the manual with automatic threshold mode U12B is turned off and the voltage from the IF GAIN control asserts itself through diode CR20 only when that level is higher than the AGC signal at the input of R14A. The digital-to-analog converter is coupled through U11D and is used to insert threshold level from a remote location through receiver control. Diversity AGC applied through transistor gate U11C to the input of U14C and to amplifier U14B influences the AGC signal only when its level is higher. When AGC dump is enabled (during certain BITE modes and local/remote operations that required dumping of AGC) receiver control enables flip-flop U9A which turns on transistor U10E. This rapidly discharges capacitor C52 thereby preventing U14A from acting as integrator.

The integrator amplifier is coupled to AGC filtering, consisting of capacitor C59, resistors R76, R77, R81 and R83, diode CR21 and amplifier U17A. If AGC dump is asserted (in certain BITE modes) transistor gate U12D is turned on providing a much faster charge path for C59 through resistor R78. The output of the filter amplifier U17A is coupled to amplifier U17B. This amplifier provides the AGC signal to IF amplifier U8. At the same time U17B provides one input to A3 AGC drive amplifier U17D through diode CR26. If ISB is installed and enabled, a second AGC signal from that circuit card is coupled to U17D through diode CR27. The two diodes bias the strongest of the two signals to the input of U17D. The output of this amplifier is coupled through J2 to AGC circuits on circuit card assembly A3.

An AF/RF meter comparator circuit is contained on circuit card assembly A4. This circuit monitors the main RF, the ISB RF and the AF that may be input from either the main or the ISB signal. The circuits consist mainly of comparator amplifiers U24A (AF), U24B (ISB-RF) and U24C (main-RF). All three amplifiers operate in the same manner with their negative inputs accepting the AF or RF reference while the positive input is referenced from the digital-to-analog converter U21. The output of each amplifier is output through connector J2 to Receiver control. From this information the microprocessor adjusts

the input to U21 which in turn adjusts the converter signal to the AGC in all modes except manual. The output of three comparators are also processed to the front panel meter readout where the RF or AF signal level can be monitored.

4.3.5 Independent Sideband (ISB), A5

The Independent Sideband (ISB) circuit card assembly A5 contains IF circuits, AF circuits and AGC circuits. The description of these circuits follows and are shown in two separate functional block diagrams in Figures 4-6 and 4-7. Input signals to the circuit card include: IF signal, BFO signal, AGC, and audio signals from A4. Output signals include AGC and audio to A4, and AGC and audio to AF OUT J3 on the rear panel, through circuit card assembly A4.

4.3.5.1 IF Circuits

Figure 4-8 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4 along with the AF function. This circuitry consists of a four stage IF amplifier, a BFO amplifier, a product detector, an audio amplifier, two audio line drive amplifiers, and AGC circuitry. The IF signal is routed from bandpass filter FL1 by the filter selection switch, located on circuit card assembly A4 to the IF amplifier on A5. This filter is selected in the ISB mode of operation, so that an IF signal is routed to A5 only in that mode. The IF amplifier is identical to the one located on A4 and is described in Paragraph 4.3.4.1. The IF signal from the AGC controlled IF amplifier is routed both to the AGC circuits and to the signal input port of product detector U11. A BFO signal from A4 is applied to the base of transistor Q7 through capacitor C30, amplified and applied to the carrier input port of the same detector. The detector removes the carrier and applies, through its audio output port, the audio signal, through capacitor C43, to an audio amplifier.

4.3.5.2 AF Circuits

Figure 4-7 shows a functional block diagram of the AF circuitry, along with the IF circuits, as they function on circuit card assembly A5. This circuitry consists of an audio amplifier and two audio line driver amplifiers. The audio signal, as received from the product detector, is connected, through capacitor C43 and resistors R78 and R79, to the base of emitter follower amplifier Q8. The output of this amplifier is then routed to circuit card assembly A4. Refer to 4.3.4.2 for a description of the ISB audio on A4. The attenuated audio signal is routed back to A5 and applied to the input of one line driver amplifier integrated in U12. The output of this amplifier drives transformer T2 with a center tapped 600 ohm output. This output is routed to AF OUT J3 on the rear panel. The main audio signal from the A4 audio is connected to the second amplifier U12 and processed in the same manner as the ISB audio except through transformer T1.

4.3.5.3 AGC Circuits

Figure 4-6 shows a functional block diagram of the AGC circuits for circuit card assembly A4. These circuits are identical to ISB AGC circuits and are described in Paragraph 4.3.4.3.

4.3.6 Serial Interface, A6A1

Refer to Figure 4-8, RS-232C Remote Control Interface Block Diagram, as an aid in understanding the following description. The Serial Interface consists of a UART, a Baud Rate Generator, an Interrupt Control and a Serial Line Interface.

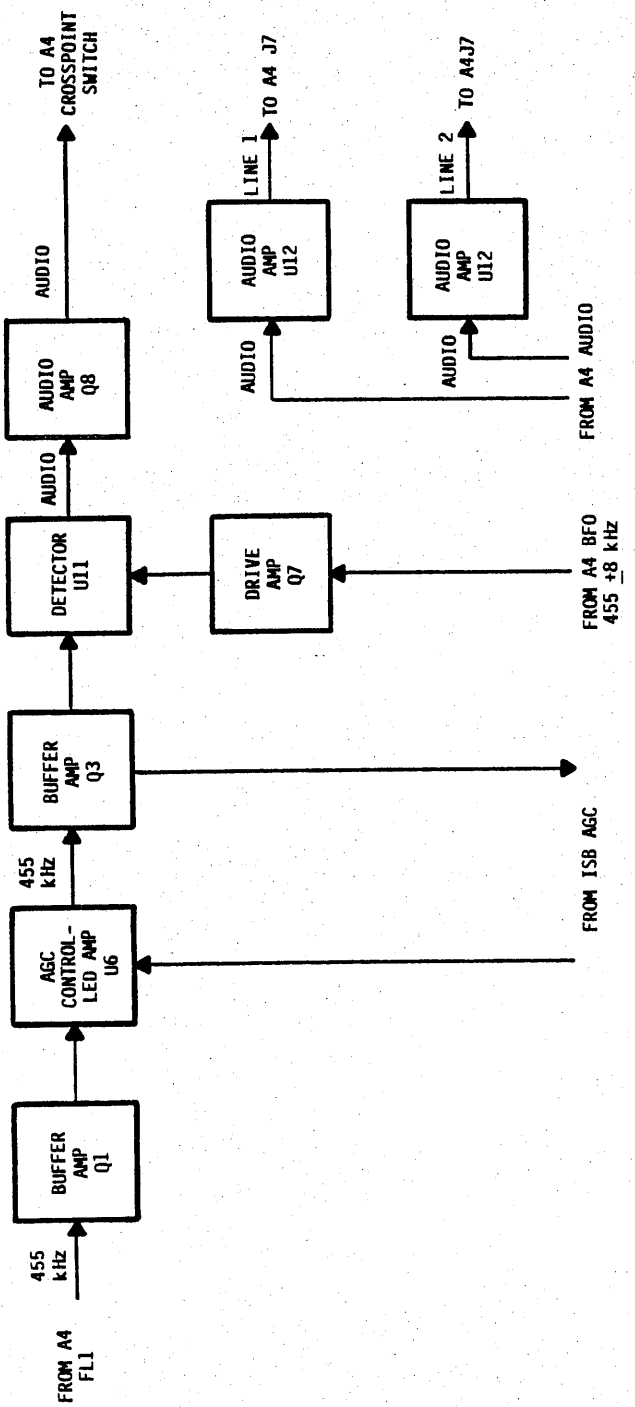


Figure 4-7. ISB Functional Block Diagram

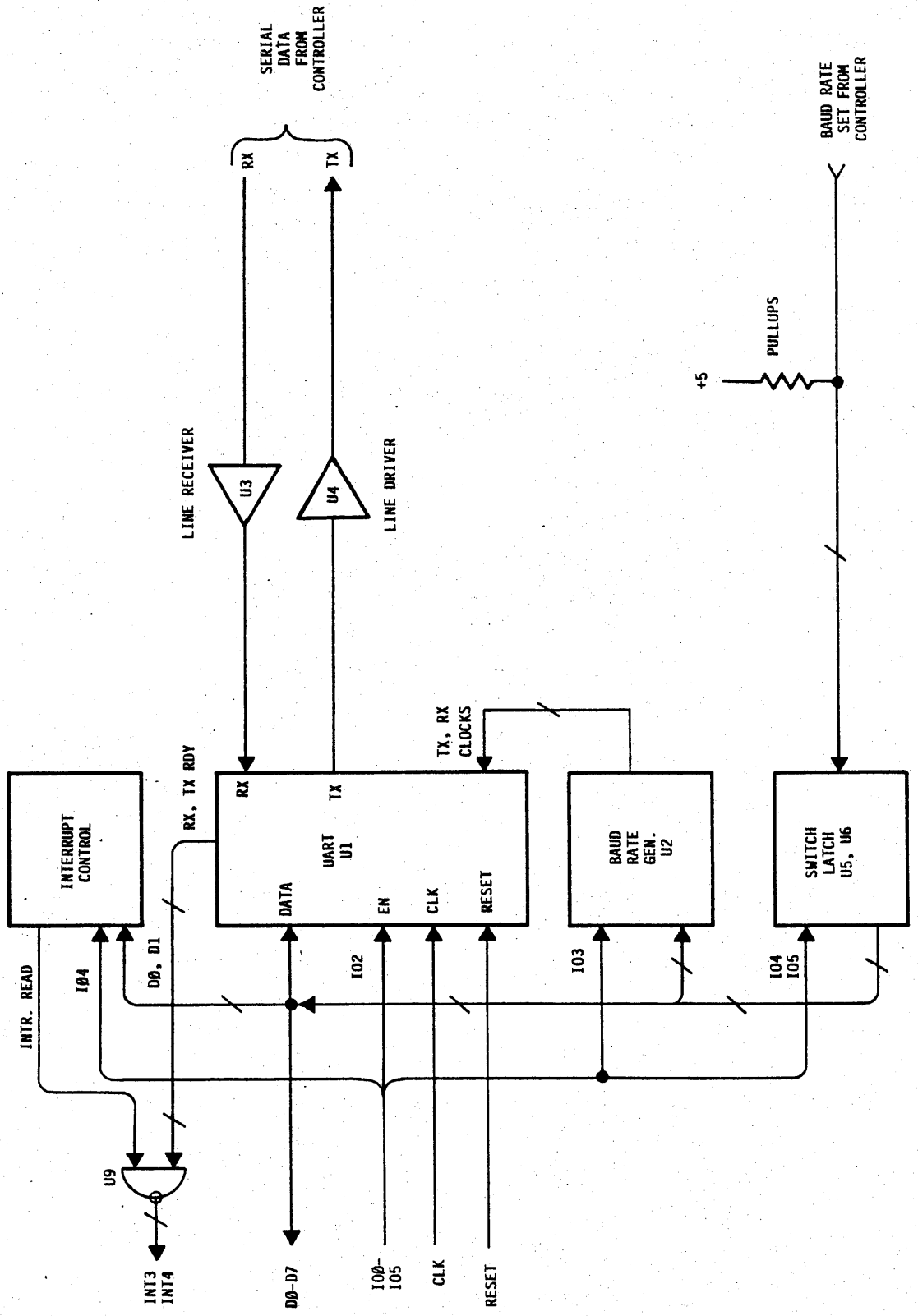


Figure 4-8. RS 232C Remote Control Interface Block Diagram

4.3.6.1 UART

The UART contains a transmit and a receive section. The receiver converts the incoming serial data stream into 8-bit parallel words and places them on the CPU data bus, D0-D7. The transmitter, when directed by the CPU, takes 8-bit parallel words from the CPU data bus and puts them into a serial format for serial transmission to the remote controller. Timing and control of receive and transmit functions is controlled directly by the CPU control bus.

The UART is initialized after the CPU is reset, under program control. Transmit and receive clocks (TX,RX) are supplied by the baud rate generator at 16 times the baud rate.

4.3.6.2 Baud Rate Generator

U2 is a programmable transmit and receive baud rate generator. This generator divides the frequency of clock oscillator U7 down to the programmed transmit and receive rates. The frequency generated by U2 is obtained from the CPU data bus upon initialization of the CPU after powerup. This data is strobed into U2 by the IO3 address line.

The CPU generates the baud rate set data from information supplied by the Switch Latch, U5 and U6. As shown in Figure 7-7A, U5 permits externally selecting the baud rate, while U6 permits externally assigning and address to the receiver. Table III is used to set pins W through Z for the desired baud. Table I is used to set pins K through T for the desired receiver address. The inputs are strobed onto the data bus by the IO4 and IO5 address bits under program control.

4.3.6.3 Interrupt Control

When data is available from the remote controller, the UART make an interrupt request by asserting the RX RDY output. The CPU, under program control, periodically enables the interrupt control using data bits D0, D1 and address IO4. U9 then passes the RX RDY signal as Interrupt 3 to the CPU. The CPU stops normal program functions and starts the interrupt routine to accept data from the controller.

When the remote controller requests data from the interface, TX RDY from the UART is asserted. The CPU enables the interrupt control using D0, D1 and I04 as above, and brings Interrupt enable high. U9 passes the TX RDY to the CPU as the Interrupt 4 signal. The CPU stops normal program functions and starts the interrupt routine to send data to the controller.

4.3.6.4 Serial Line Interface

U3 is a differential to single ended line receiver. It converts RS-232 and RS-422 compatible signals to TTL level signals suitable for driving the UART. U4 is a single ended to differential line transmitter. It converts TTL level signals from the UART to RS-232C and RS-422 compatible signals suitable for serial transmission to the remote controller.

4.3.7 IEEE-488C Interface Module, A6A1 (Optional)

Refer to Figure 4-9, IEEE-488C Interface Block Diagram as an aid in understanding the following description. The remote control interface circuit consists of circuitry which includes; an address switch, the IEEE-488C interface bus transceivers, the general purpose interface adapter (GPIA), and the microprocessor interrupt circuitry. The address switch

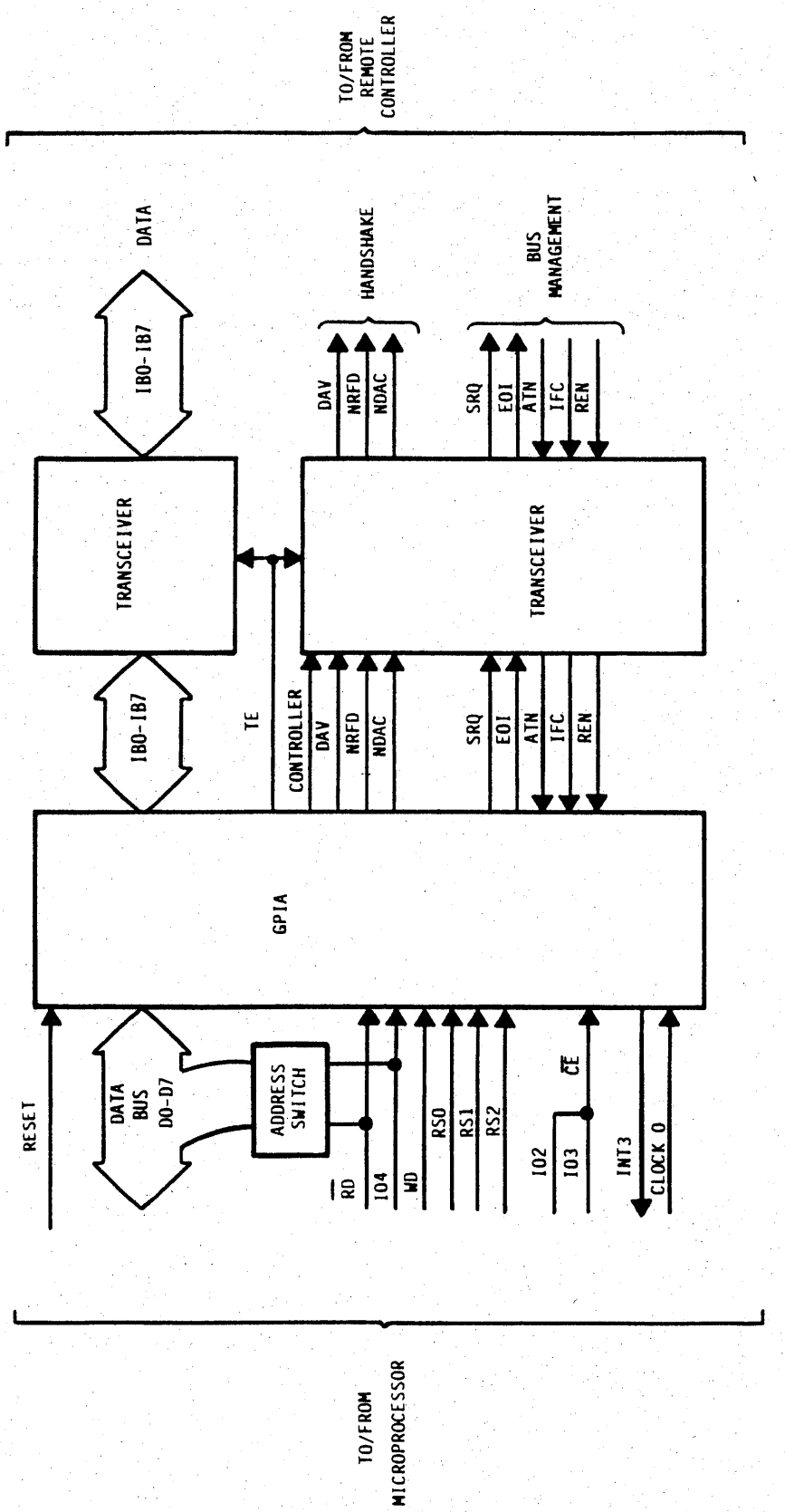


Figure 4-9. IEEE-488C Interface Block Diagram

sets the receiver address. Transceivers provide compatible bi-directional connections to the IEEE-488C interface bus. The GPIA initiates an interrupt request upon receipt of the receiver address from the remote controller/computer. The interrupt circuitry requests the interruption of the microprocessor processing and directs the microprocessor to an interrupt vector address for a specific interrupt routine. Figure 7-7 is a schematic of the remote control interface circuit.

The IEEE-488C remote control interface circuit card assembly provides an electrical interface for communication with a remote controller/computer via a suitable interface bus. In addition, interconnections between the receiver and the remote controller/computer are made through a multi-pin remote control interface connector A6A1J2, located on the modified receiver rear panel. Refer to Figure 2-7.

Communication between the remote controller/computer and the modified receiver is achieved through messages composed of data words (bytes) in serial strings. Each string of data is prefixed with a primary address for talker and/or listener operation (MTA or MLA byte). To initialize communication, the remote controller/computer sends a binary address code to the modified receiver. This binary address must be preset on a miniature five-pole address switch assembly (A6A1A1S1), located on the IEEE-488C remote control interface circuit card assembly and accessible from receiver rear panel, before installation of the equipment.

The IEEE-488C remote control interface circuit comprises three functional elements which include; a bus driver/receiver circuit, general-purpose interface adaptor (GPIA) circuit, and microprocessor interrupt circuit. This circuit implements control operations utilizing eight data lines DI01-DI08, three handshake lines DAV, NDAC and NRFD, and five bus-management lines EOI, IFC, SRQ, ATN and REN. Detailed information on the IEEE-488C remote control interface is contained in the specifications publication IEEE-STD-488C-1978 (the IEEE Standard Digital Interface for Programmable Instrumentation). Copies are available from the IEEE, 345 East 47th Street, New York, NY, 10018.

4.3.7.1 General Purpose Interface Adapter (GPIA) TMS9914A

The IEEE-488C interface bus lines, through the transceivers, connect to their corresponding terminals on the GPIA (U1). Microprocessor connections are made through connector J1 to the GPIA. These connections include data lines DØ-D7, clock Ø, read ($\overline{RD}$), write ($\overline{WD}$), and chip enable ($\overline{CE}$). Initialization of the GPIA is activated through the $\overline{RESET}$ line. GPIA operation is controlled through fourteen internal registers which are written on and/or read out by the microprocessor, being addressed through $\overline{CE}$, RSØ, RS1 and RS2.

4.3.7.2 Addressing and Interrupt

When the remote controller/computer sets the ATN line true and sends the receiver address on the data lines DI01-DI08, the GPIA recognizes this and gives an output on the $\overline{INT3}$ terminal. This inititates an interrupt request which is a request to the microprocessor to stop normal processing and to force processing to an interrupt routine which will consider that data being received.

4.3.7.3 Listener Operation

The remote control interface circuit acts as a listener while waiting to be addressed by the remote controller/computer and when directed by the microprocessor during a microprocessor routine. During these times, the GPIA output TE and sets the

transceivers (through their SR inputs), so that the remote control interface circuit accepts remote controller commands and data from the IEEE-488C interface bus. Here, data on lines DI01-DI08 is sent directly through to the GPIA from the remote controller/computer, and the handshaking line DAV (data available) signal is sent directly through from the remote controller/computer to the GPIA, while handshaking lines NRFD (not ready for data) and NDAC (not data accepted) signals are sent directly through from the GPIA to the remote controller/computer.

The GPIA acts on the data and/or sends it on to the microprocessor. It also performs the required handshaking protocol with the remote controller/computer, as directed by the microprocessor, through the GPIA internal registers.

4.3.7.4 Talker Operation

The remote controller/computer addresses the remote control interface circuit to talk by placing the talk address of the circuit on data lines DI01-DI08 with the ATN line true. The GPIA decodes the data as its talk address and requests status information from the microprocessor. Data is transferred from the microprocessor to the GPIA. The GPIA TE sets the transceivers so that the remote control interface sends data from the GPIA on to the IEEE-488C interface bus and thus to the remote controller/computer. Here, data on lines DI01-DI08 is sent directly through from the GPIA to the remote controller/computer, and the handshaking line DAV signal is sent directly through from the GPIA to the remote controller/computer while handshaking lines NRFD (not ready for data) and NDAC (not data accepted) signals are sent directly through from the GPIA to the remote controller.

The GPIA transfers data from the microprocessor to the remote controller/computer and also performs the required handshaking protocol with the remote controller/computer as directed by the microprocessor.

4.3.7.5 Bus Management Lines

ATN, IFC, REN, SRQ and EOI are the IEEE-488C interface bus management lines. ATN, IFC and REN have their associated transceivers hardwired for direction of signal flow from the remote controller/computer to the GPIA only. As indicated earlier, ATN is set true by the remote controller/computer when it wants to clear lines to send a message. IFC is used by the remote controller/computer to set the interface system into a known quiescent state. REN is used by the controller/computer to select one of two alternative sources of device programming data, local or remote. EOI is bidirectional, controlled by the GPIA, and is used to indicate the end of a message either to the remote controller/computer or the remote control interface circuit.

4.3.7.6 Bus Transceivers

The sixteen bus lines from the remote controller/computer are applied through connector J2 and enter the two quad transceivers U2 and U3. Signal flow direction through each line in the transceivers is determined by a TE output from U1, (Transmit Enable).

4.3.7.7 Command Structure for Service Request (SRQ)

Using the protocol as defined in IEEE-488C for Serial Request Functions the receiver generates a serial request to the controller under the following conditions:

1. Receive data error.

2. Receiver synthesizer out-of-lock.

3. Signal acquired (in stop on scan on stop on sweep mode).

4. Signal lost (in stop on scan on stop on sweep mode).

In response to serial poll request from controller the equipment will transmit, serial status byte of the following structure.

SERIAL POLL STATUS BYTE

MSB							LSB
CHANNEL AQUISITION STATUS CHANGED	1			RECEIVER ERROR *			

*Receiver error could be caused by a synthesizer out of lock, or the remote I/O system interpreting input data as incorrect (such as out of range).

Receive data error = 01001000
Receiver synthesizer out of lock = 01001000
Signal required = RX: SRQ 192 (11000000)
Controller "? L_F"
RX: "C23@F12,34·····E1L_F"
Signal Lost = RX: SRQ 192.(11000000)
Controller "?L_F"
RX: "C23QL_F"

NOTES: 1. RX Scanning In Remote Q1 Mode -Stops on initial acquisition only and on loss of signal. Controller must command receiver to continue. (Pa)

2. RX Sweeping In Remote Q1 Mode - Stops on signal acquisition. Controller must command receiver to continue. (PSa)

4.3.8 Microcomputer, A6A2

Refer to Figure 4-10, Microcomputer Block Diagram, as an aid in understanding the following description. The Microcomputer consists of a CPU, ROM, RAM, a Data buffer, and Address Decoder, a Port Decoder and Interrupt Control logic. The Microcomputer controls the receiver by reading the operating program in ROM and routing data and control signals to the receiver via an eight-bit data bus. This bus is common to major receiver control circuitry and is the primary means of communication between the Microcomputer and the receiver.

4.3.8.1 CPU

The CPU is a Z-80 chip. A 2 MHz clock signal is provided to the CPU by a 4 MHz crystal oscillator and divide by two circuit. The CPU controls a 16-bit address bus and an 8-bit data bus. It also outputs the RD, WR and other control signals necessary for I/O control. The CPU performs instructions which are obtained from the control program contained in ROM. These instructions are routed from ROM to the CPU instruction register via data buffer, U8, and then carried out during instructions cycles. Each instruction cycle specifies the functions to be performed by the rest of the Digital Control section. The CPU reads and writes data to the RAM and 8-bit buffered data bus on A9A2 via the IODO-IOD7

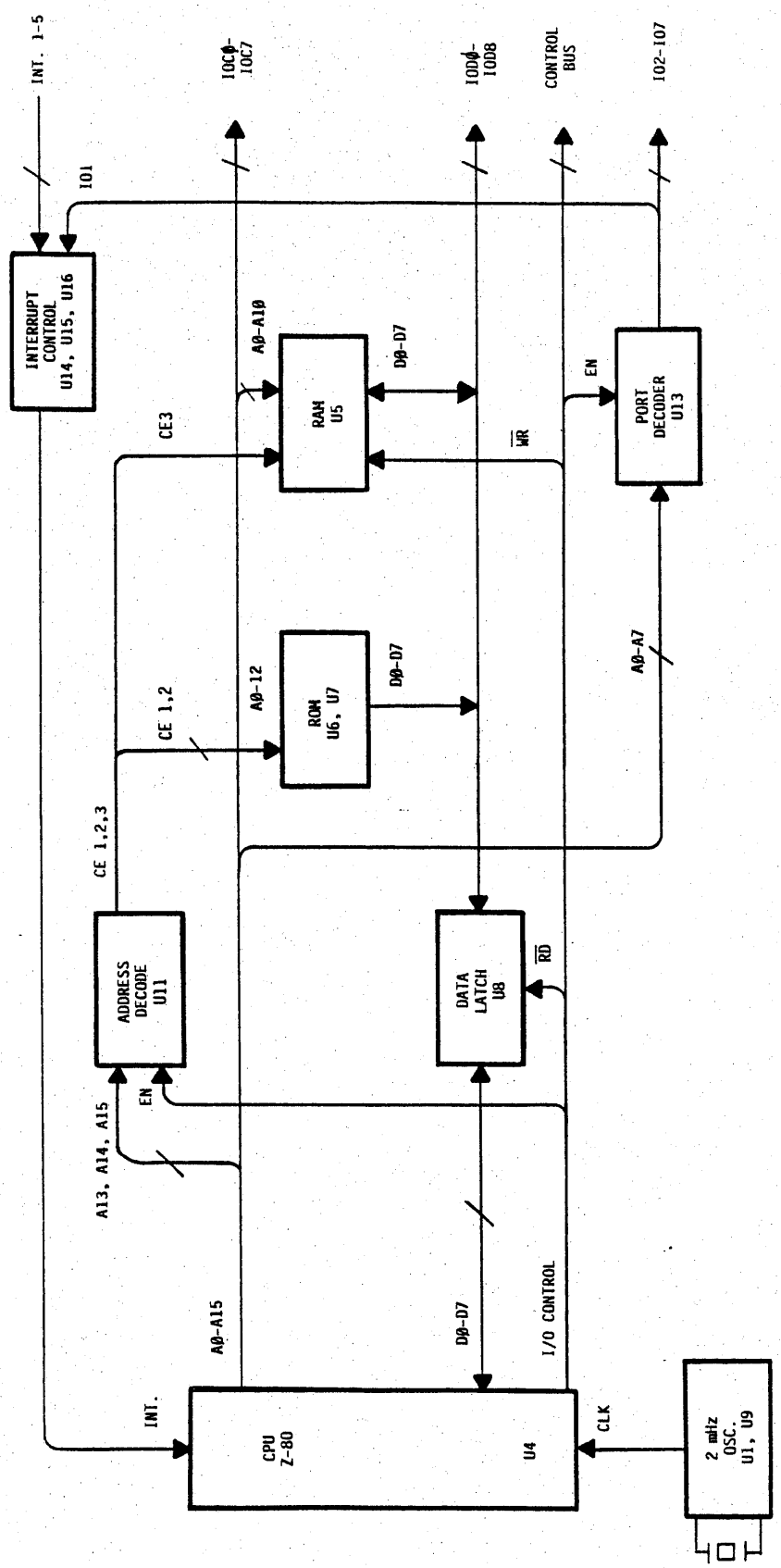


Figure 4-10. Microcomputer, A6A2, Block Diagram

bus the CPU specifies the device written to or read from via the IOC0-IOC7 bus. Address and data movement is coordinated by the CPU via the I/O control line.

4.3.8.2 ROM

The operating control program is stored in ROM, U6 and U7. These are type 2732 or 2764 EPROMS. Each of these units contains either 4K or 8K 8-bit words for a total of 8K storage (2732) or 16K storage (2764). The ROM is directly addressed by twelve bits of address from the CPU. Address decode U11 enables ROM via the address bits A13-A15 from the CPU. Thus, the ROM, when addressed and enabled, places 8-bit instruction words directly on the CPU data bus, IOD0-IOD7.

4.3.8.3 RAM

The RAM consists of one 6116 random access memory chip. It contains 2K 8-bit words. The RAM is addressed directly by 10 address bits from the CPU. Address decode U11 enables the RAM via the address bits A13-A15. The RAM is bidirectional, inputting data when WR is low and outputting data when WR is high. Thus, the RAM, when addressed and enabled, places data on the CPU data bus or accepts data from the CPU data bus.

4.3.8.4 Data Buffer

The data buffer is a bidirectional data buffer. When the RD control line is high from the CPU, the data buffer transfers data from the CPU to the IODO-IOD7 data bus. When RD is low from the CPU, the data buffer transfers data from the IODO-IOD7 data bus to the CPU.

4.3.8.5 Address Decoder

The address decoder is used by the CPU to select either ROM or RAM. The upper three bits of address, A13-A15, are decoded to produce CE1 or CE2 for ROM select or CE3 for RAM select. The address decoder is enabled by the MREQ control line from the CPU.

4.3.8.6 Port Decoder

The port decoder latched outputs IO2-IO8 provide the I/O strobe for selection or addressing of the various elements of the front panel and receiver control circuitry. These outputs are used in conjunction with the 8-bit buffered data bus to send or receive data. The selected addresses are latched into the port decoder output from the CPU address bus, under program control, and are enabled by the I/O control line.

4.3.8.7 Interrupt Control

The interrupt control permits one of five external interrupt conditions to flag the interrupt line to the CPU. U16 is the interrupt "OR" circuit. When any of the five interrupts (INT3-7) goes low, the interrupt line to the CPU goes low. The CPU responds by executing the interrupt routine stored in ROM. IO8 from the port decoder is brought low, transferring the interrupt word through U15 to the data bus, and then to the CPU. The interrupt word is read by the CPU which then executes the proper program routine to service the interrupt. U14 is a counter/timer which establishes a 500 microsecond interrupt interval.

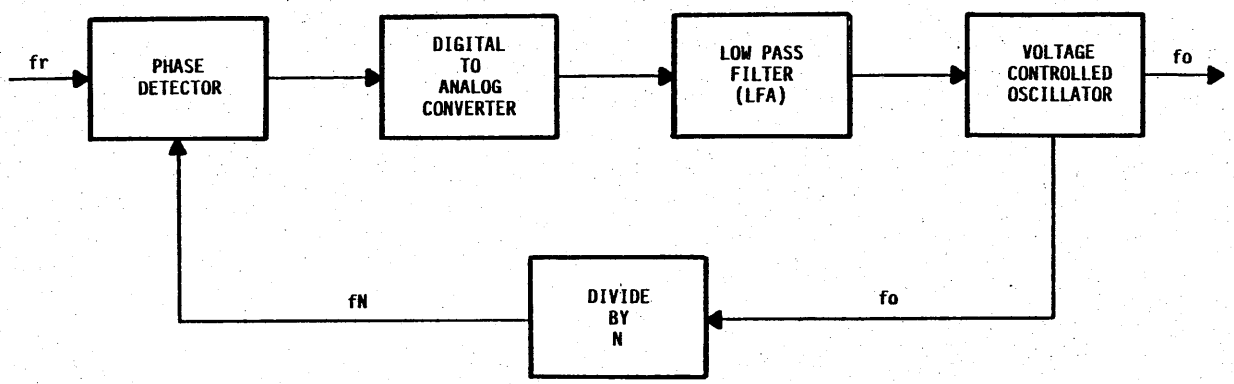
4.3.9 First Local Oscillator Synthesizer, A7

The first local oscillator synthesizer circuit card assembly A7 contains circuits to produce the first oscillator frequency of 40.955 to 70.454999 MHz for the first mixer which in turn produces the first IF signal of 40.455 MHz. The description of this circuitry is divided into three basic groups: operation of phase lock loops, the digital control circuitry and the oscillator control circuitry. Figures 4-11 through 4-13 respectively, show simplified block diagrams of the three basic circuit divisions. Input signals to the circuit card assembly include receiver control and a 1 MHz reference frequency. The only output signal from the assembly is the 40.955 to 70.454999 MHz oscillator signal.

4.3.9.1 Operation of Phase Lock Loops

A basic phase lock loop consists of essentially four main blocks. These are shown in Figure 4-11 and are a Voltage Controlled Oscillator (VCO), a divider capable of dividing the output of the VCO by an integer number (- N), a phase detector (Ø), a digital-to-analog converter and a Loop Filter Amplifier (LFA). A phase lock loop configured in this manner is capable of locking to the incoming reference frequency (F ref) and in discrete steps, each frequency step being the same as the incoming reference frequency (F ref). This is derived from the fundamental formula for this type of loop which is Fo = F ref x N; therefore, to vary the main VCO Frequency (Fo) either Freq or N would have to be changed. Most loops perform frequency change by modification of N, the integer divide ratio. It is noted, however, that this type of simple single loop can only vary in frequency steps as small as the reference frequency (F ref). However, it is assumed that a system is possible whereby the main oscillator (Fo) frequency can effectively divide a fractional number, in which case it is possible to achieve a much finer resolution, given the same higher frequency reference. Assume that Fo is 50.123467 MHz and the reference frequency is 100 kHz. Then, using the above formula, the result is with n as the ratio, a non-integer number: 50.123467 = 0.1 x n; therefore, n = 501.23467. If we split this number into its integer part and its decimal part, the result is a three decade integer and a five decade decimal number. Generating the non-integer part as an actual frequency is done by considering a portion of the frequency spectrum of interest between 50.1 MHz and 50.2 MHz, where this finally generated frequency will occur. Thus, it is possible to generate any signal between these two frequencies by an averaging technique, that is to say (see Figure 4-12) if the signal at 50.2 MHz is sampled, 23,467 times and the signal at 50.1 MHz, 76.533 (100,00-13,467) times then the average or apparent signal produced by this sampling would occur at the frequency of interest at 50.123467 MHz. This type of sampling produces a large number of sampling sideband on the main output frequency. These can be removed, however by producing a signal equal and opposite to these predictable sidebands and adding this to the oscillator control signal effectively nullifying the production of these sidebands.

In the synthesizer used in the Receiver the circuitry can be split in two parts: for the operating analysis, those circuits involved in the generation of the digital signals to control the generation of the 5-decade decimal part of the divide ratio number, n (which in turn controls the sampling technique and the signal to sum with the oscillator control signal), and those circuits including an oscillator, 3-decade integer divider, phase detector, summing amplifier and lowpass filter (making up the components of a simple phase lock loop). These two parts in further discussions will be referred to as the Digital Control and the Oscillator Control Circuitry. A separate section is included for auxiliary circuitry which is provided to produce large frequency step control and out-of-lock indications for the receiver.



NOTE:

FOR NORMAL OPERATION fo = fr x N

WHERE:

fo = OSCILLATOR FREQUENCY
fr = REFERENCE FREQUENCY
N = DIVIDE BY NUMBER

Figure 4-11. Typical Phase Lock Loop Functional Block Diagram

4.3.9.2 Digital Control

Figure 4-12 illustrates a simplified block diagram of the digital control circuitry. The circuitry associated with the time control, the incoming 1 MHz reference signal from A7J2, is used as the clock for accumulator and registers through the NOR gate U4D which drives U20, U21 and U22, and is routed directly to U3, U5 and U18. The Hex D flip-flops U3 and U5 with U1A and U1B provide a 10-level ring counter. This counter is used to provide timed pulses to clock the accumulator from first accumulation to second accumulation and sequentially clock out the data in the latches U8 through U12 to the full adder U15. Flip-flop U3 provides a pulse that is 1 clock pulse wide but is delayed 5 pulses from DØ (the input) to Q1 (the output). The output at U3Q4 is connected to the input DØ of U5. U5 also provides 1 clock-pulse-wide pulses but each output QØ through Q4 is used to drive the incoming data latches. U4A and U4B converted the narrow pulses from U3/QØ and U5/QØ into a 50% duty cycle square wave with a period of 10 clock pulses (each half cycle being 5 clock pulses long). The 180° out-of-phase outputs at U4A pin 1 and U4B pin 4 provide control to U2A, U22, U19A and U19B to ensure that these devices are enabled during the correct half cycle. The 100 kHz reference for the reference side of phase comparator is taken from U5 output (Q4). U5 output (QØ) is provided to U4C via U7C to reclock the CARRY IN to U15 and also to U6 to provide the clock for alignment of signals out of the HEX D flip-flop U6.

In serial-to-parallel conversion, the incoming serial data stream from the A9 Receiver control assembly consists of DATA, CLOCK and STROBE signals. The strobe is routed to U6 input D1, where its output is reclocked. This output at U6 Q1 is fed back to D2 and its output (Q2) provides a strobe input to U13 and U14 one clock pulse delayed. The incoming CLOCK is fed to U14 through U8, in parallel. The serial DATA is fed first into U14, which from its output on U14 pin 10 to U12 and U13 shift registers. The output from U12 at pin 10 is fed to U10 and U11, and so on to U9 and U8 to complete the data load and form the serial-to-parallel conversion of synthesizer data into the data registers. The data registers U8 through U14 hold the data for the synthesizer frequency, the U8 register holding the 4-bit BCD data for the synthesizer frequency, the U8 register holding the 4-bit BCD data for the 1 Hz digit and each register the next decade up (the U9 register holding the 10 Hz data, and so on) to the U14 register, which holds the 1 MHz and 10 MHz data.

If the front panel RF frequency is set to 10.426800 MHz then the actual loaded data is 39.255 MHz above this frequency, which is 49.680800. The first IF frequency is 40.455 MHz, so we can see that a further offset of 1.2 MHz less than the main LO frequency of 50.881800 is introduced by the microcomputer into the serial data stream sent to A7. This is accounted for in the actual mathematical process in the first and second accumulator circuitry, which replaces this offset before generating the final VCO control voltage to the local oscillator.

With accumulator operation, the data loaded into the registers U8 through U12 is fed in 4 parallel boards under control of the ring counter U5 during the first half cycle of the tuning (as discussed in the tuning section) to the Full NBCD Adder U15. As the accumulation proceeds, the accumulating sum is passed from the sum outputs of U15 to the 4-bit wide latch U18. The Carry Out signal from U15 is also stored in U18, then clocked out to U7A. It is then placed under control of U7C from the tuning circuits, flowing through U4C back into the Carry-In port of U15, deriving the first accumulation. The outputs from U18 will be fed into the 4-stage shift registers contained in U20 and U21. U20 and U21 are 18 stage registers each divided into 2 four-stage registers and 2 five-stage registers. The four outputs from U18 are fed into the 4-stage registers in each half of each U20 and U21 and then the output of these 4-stage registers is fed back to the 5-stage register in each half of U20 and U21. At the end of the first accumulation the data at the output of the 4-stage register appears at the input to the tri-state 4-bit buffer U2A.

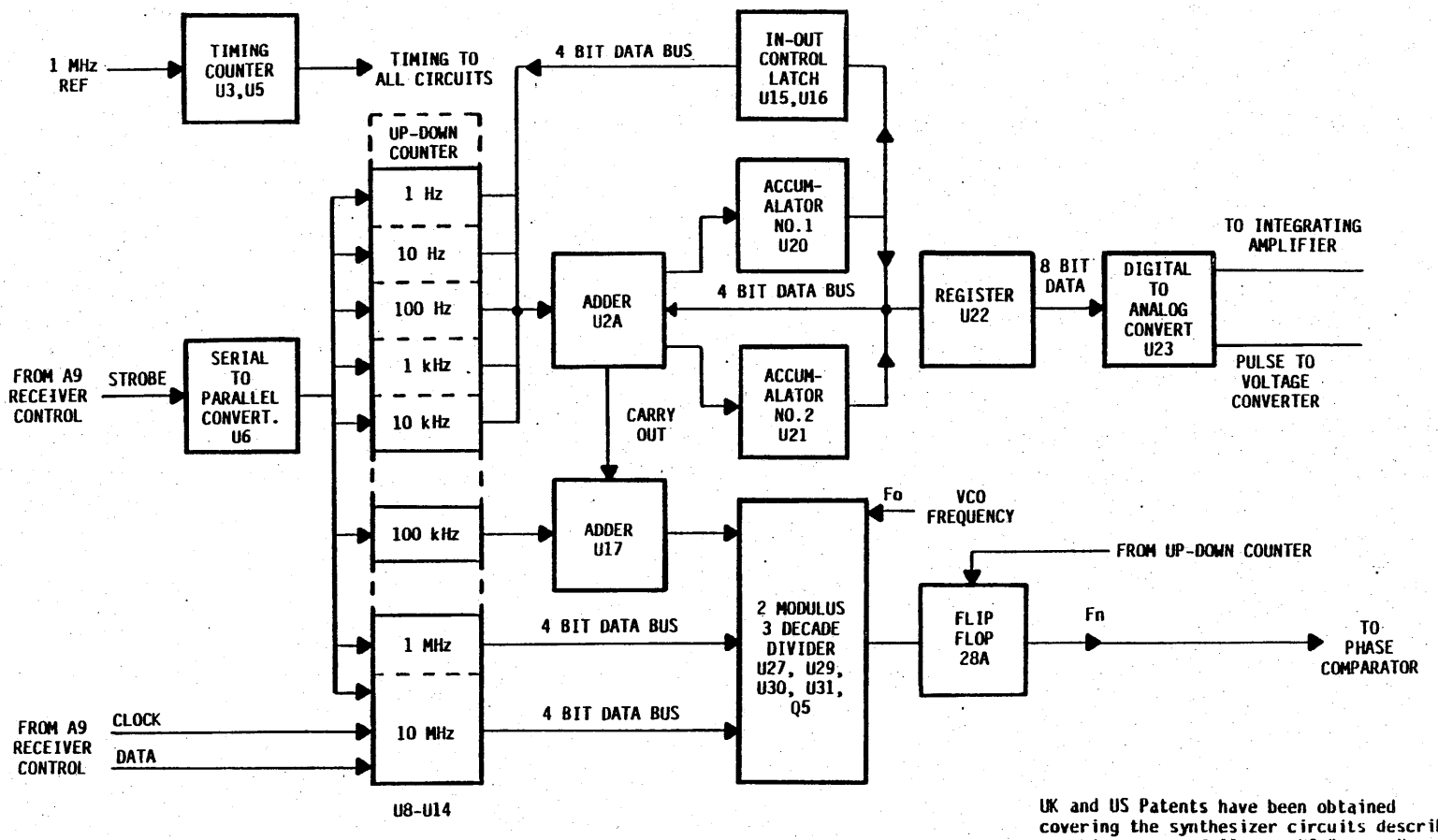


Figure 4-12. First Local Oscillator Digital Circuits Functional Block Diagram

As the second accumulation begins U2A is enabled, under control of U4A, and the data at its inputs is transferred to the B inputs of U15 and NBCD Adder. During the five clock periods of the second accumulation the data in U20 and U21 is shifted back to the B inputs of U15. During this period, the data in U8 through U12 is held as the tri-state output enable mode of these registers is not enabled, ensuring that the results of the first accumulation are added again in the second accumulation. At the end of the second accumulation the results of the first accumulation will be propagated through the 5-stage register in each half of U20 and U21 and will appear at the inputs DØ through D3 of the 4 x 4 Multiport Register U22, and at the A1 through A8 inputs to U15. If no new data is loaded into U8 through U12 from the serial input data stream, then the two cycles of accumulation will continue by first accumulating the contents of U8 through U12 on one half cycle with the data at A1 through A8 in U15, and then on the second half cycle by adding the results from the first accumulation back into the B inputs of U15. Temporary storage for the results of each accumulation is provided by U18, U20 and U21.

If the result of adding numbers in U15 is a terminal count, the adder will produce a Carry-Out pulse at U15 pin 6, reset to zero and start counting again. In a real situation this process is ongoing and the adder is continually providing carry-out pulses. (See Figure 4-13, line B.) This Carry-Out pulse is fed to U6 to be reclocked. The reclocked output at U6 pin 7 is routed through U1C to a further adder U17. The carry out is also clocked by U19A so that if it occurs on one edge of the accumulating half cycle controlled from U4B, it will appear at the Q output of U19A and after reclocking in U6 through the fifth latch it is applied to the carry input of the 4-bit full adder U17. (See Figure 4-13, line C.) The adder U17 continually updates by addition (based on the carry out information from U15) the 100 kHz frequency information provided by the input storage register U13. The addition in this adder is continuous so that the outputs at U17 pins 10 through 13 are constantly changing to provide the averaging action previously discussed.

For DAC control, a 4 x 4 multiport register U22 provides storage for the results of the constant accumulations and provides the information to the digital-to-analog converter U23. U19B divides the accumulator control signal by two so that all four registers in U22 can be loaded. The read cycles to these registers are controlled by the RØA, RØB, R1A and R1B inputs of U22. The RØA and RØB inputs are fixed and the R1A and R1B inputs are controlled by the output of U19B so that during two accumulations R1 is loaded, each register RØ and R1 consisting of two 4-bit data storage areas. The data stored is that which appears at the data inputs of U22, DØ through D3. This stored information is transferred to the register A outputs and register B outputs when W Enable is high and either WØ is high in transferring RØA and RØB contents or W1 is high in transferring the contents of R1A and R1B.

The digital-to-analog converter provides an output based on the changing data at its inputs as a voltage ramp whose amplitude and DC offset are modified by the adjustment of R5. The D/A also provides a reference source for the pulse-to-voltage converter U33B.

NOTE

The pulses demonstrated in Figure 4-13 can be reproduced in circuit if the RF front panel frequency is set to 1.046000 MHz. This ensures that the accumulations start from a zero condition. B will then be at TP3, C at TP4 and E at U23, pin 2 (the D/A output).

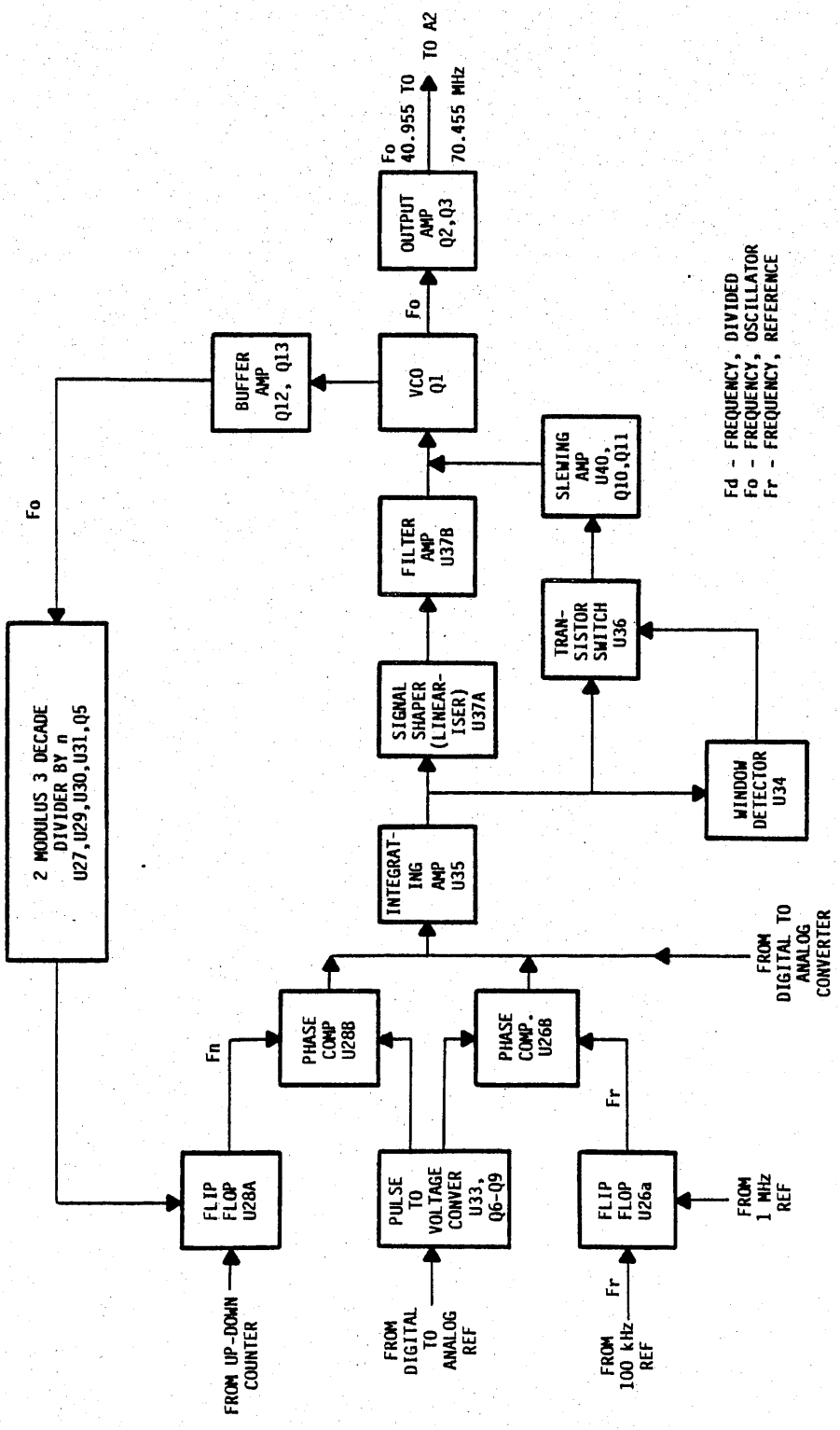


Figure 4-13. Detailed Timing Diagram

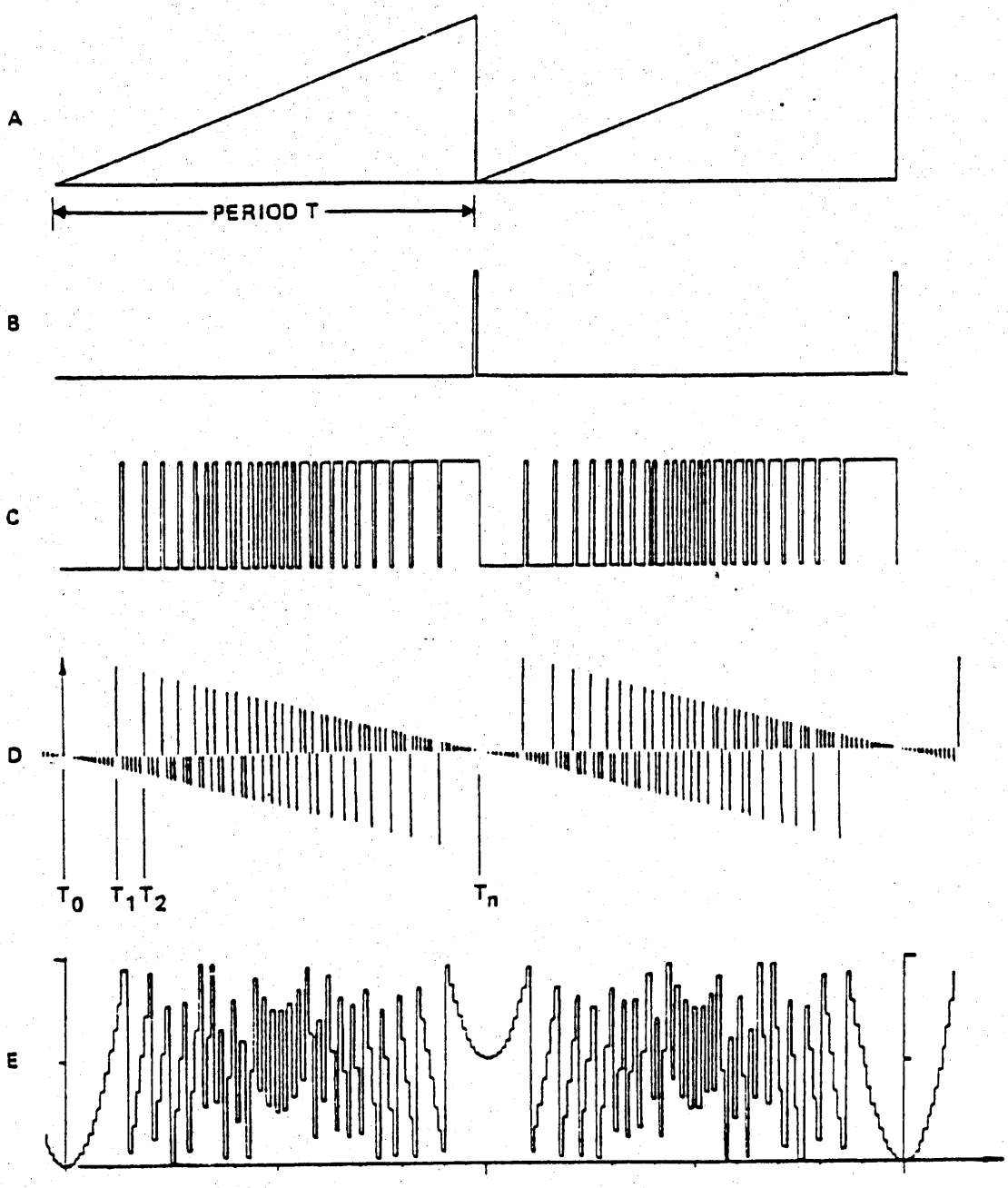
4.3.9.3 Oscillator Control

Figure 4-14 presents a simplified block diagram of the oscillator control circuits. To more fully understand the operation, the following description is divided into four principal areas: (1) Main Division, (2) Phase Comparator and Pulse-to-Voltage Converter, (3) VCO and Analog Control Circuitry, and (4) Speed-Up and Out-of-Lock Operation.

1. Main Division - The BCD data outputs for 100 kHz, 1 MHz and 10 MHz provided by U17 and U14 are applied to a 2-modulus, 3-decade divider consisting of U27, U29 and U30 and U31. This form of division ensures that by using a 2-modulus high speed control device that can divide by 10 or 11 under control of its M1 and M2 input control (27), a high-frequency input can be divided by an integer value. The terminal count from U29 is applied in inverted form by Q5 to this control input of U27. The resultant divided signal at pin 9 of U29, U30 and U31 is applied to a TTL-to-ECL converter network consisting of R30, R31 and CR7, to a flip-flop U28A. This flip-flop reclocks the divided output under control of the clock signal on U28A pin 6 from the ECL output of U27 pin 8, and then applies it to one side of the phase comparator from its quadrature outputs on pins 2 and 3.

2. Phase Comparator and Pulse-to-Voltage Converter - The phase comparator reference is derived from the 100 kHz signal from U5 pin 12, reclocked against the 1 MHz reference in U26A. The reference output at U26A pin 2 is applied to the other side of the phase comparator, consisting of U28B, U26B and U32. The ECL comparator provides phase comparator outputs at TP7 and TP8. The variable input from U28A pin is applied to a pulse-width detector consisting of CR9, CR10, Q6 and U33B. As the pulse width changes with the frequency varying from 40.455 MHz to 70.454999 MHz, the voltage at the emitter of Q6 varies continuously and linearly over a range of approximately 1 volt. The DC offset of this voltage is determined by the D/A ref from U23. U33A and Q8 from one-half of a current source to CR12 and CR14 and Q7 and Q9 from the bottom half of this current drive through CR13 and CR15. Phase-compared outputs at TP7 and TP8 are fed into the diode network formed by CR12, CR13, CR14 and CR15 and an output from this pulse-to-current converter is fed to R60.

3. VCO and Analog Control Circuitry - The current output of the phase comparator is combined with the voltage ramp from the D/A through C80. This combined signal is then applied to an integrating amplifier U35. In normal operation, the output of U35 is sent to a signal linearizing/inverter circuit U37A and to the out-of-lock window detector comprising U34C and U34D. (This is described in more detail in the speed-up and out-of-lock circuit operation.) The output of U37A at TP10 is a DC voltage that can vary from a high voltage up to 18 volts and a low voltage equal to 1 volt; it will be high when the selected frequency is at 30 Hz and low when the system requires 0.5 MHz. This DC voltage is then passed through U37B which, along with its associated resistors and capacitors, forms a low-pass filter. This output is then buffered from the VCO by resistor R88 between TP11 and TP12. A further lead-lag network is in the VCO control line between TP12 and ground, formed by R92, R93, R94 and C98. This voltage is then applied to the VCO control varactors CR3 and CR4 through R85 and L4. A voltage applied to CR3 and CR4 will vary the capacitance across the main VCO coil L5 and thus vary the frequency generated. Q1 is the main LO active device, and an output from its drain is capacitively coupled to a buffer amplifier of the cascade type, formed by Q12 and Q13. The output of this feeds the 2-modulus divider controller U27. A further output from the oscillator coil is tapped off and provides the main LO output through Q2 and Q3 with step down transformer T1.



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 4-14. First Local Oscillator Analog Circuits Functional Block Diagram

4. Speed-UP and Out-of-Lock Operation - When a large step of frequency change is introduced on the front panel (or from the remote control data bus), the window detectors U34C and U34D act as comparators, comparing the inputs on pins 9 and 10 from the VCO control circuitry with fixed high and low references on pins 11 and 8. If the voltage goes higher or lower (frequency step up or down) than these references a pulse will appear at the comparator outputs on pins 13 and 14. This pulse is applied through an RC network to a voltage converter consisting of U34B and CR19 and CR20. This voltage-offset pulse is then used to drive three switches: U36B, U36C and U36D. These switches bypass the lowpass filter U37B and increase the integrating bandwidth of U35 and one switch, providing a feed forward from TP10 to the positive input of U40. U40 provides an integrated drive to push/pull drivers Q10 and Q11. These drivers provide high-speed charge or discharge of C98 (through R91, C97, and R94). When the control voltage approximates the correct voltage for the frequency selected, this circuit becomes operative. U34A provides the Out-of-Lock signal for feeding to the A9 Receiver control board and then to A6A2 for processing. If a pulse or a constant low level is applied to pin 6 of U34A its output will then go low, indicating OOL.

4.3.10 Second LO and BFO Generator, A8

The second local oscillator (LO) and beat frequency oscillator (BFO) circuit card assembly contains the circuitry for these two oscillators. (An internal/external frequency reference circuit is also contained on this circuit card.) The second local oscillator develops the fixed 40 MHz 2nd LO signal for the second mixer. The BFO is a variable oscillator that provides the basic 455 kHz beat frequency for sideband (SSB) and CW modes of operation. The oscillator, through receiver front panel control, may be set either at 455 kHz or varied 8 kHz on either side of its basic frequency for CW operation. The internal/external frequency reference circuit provides a reference frequency for both oscillators' phase lock loops as well as the first LO contained on A7. In addition, the circuit includes an internal temperature-controlled crystal oscillator which supplies a selectable 1 MHz, 5 MHz or 10 MHz reference frequency output at the rear panel. An external reference frequency can be used in place of the internal reference. The circuit description for the internal/external reference, the second LO and BFO are described under their respective headings, with functional block diagrams shown in Figures 4-15 and 4-17.

4.3.10.1 Internal/External Reference Frequency

The A8 circuit card contains circuitry that permits either an internal or external reference frequency. This reference frequency is required for the operation of all three oscillator synthesizers. A reference in/out connector and switch on the rear panel, in addition to linkage on the A8 circuit card, provide for the selection of either internal or external frequency and for selecting the proper divide-by-N frequency for the Phase Comparator.

4.3.10.2 Internal Mode

A 5 MHz crystal oscillator Y1, located on A8, is used as the internal reference frequency. With the rear panel REF INT/EXT switch in the INT position, the base of Q1 is grounded through R7, which turns voltage regulator U1 on. The voltage from this regulator enables the temperature controlled crystal oscillator. Approximately 30 minutes are required for maximum stability. The oscillator output is coupled through capacitor C5 to the base of transistor switch Q5. With the ground applied through the INT/EXT switch, the base of Q5 is held high through inverter U2A and diode CR3 while the base of transistor switch Q4 is held low through diode CR2. Transistor Q5 conducts, transferring the 5 MHz

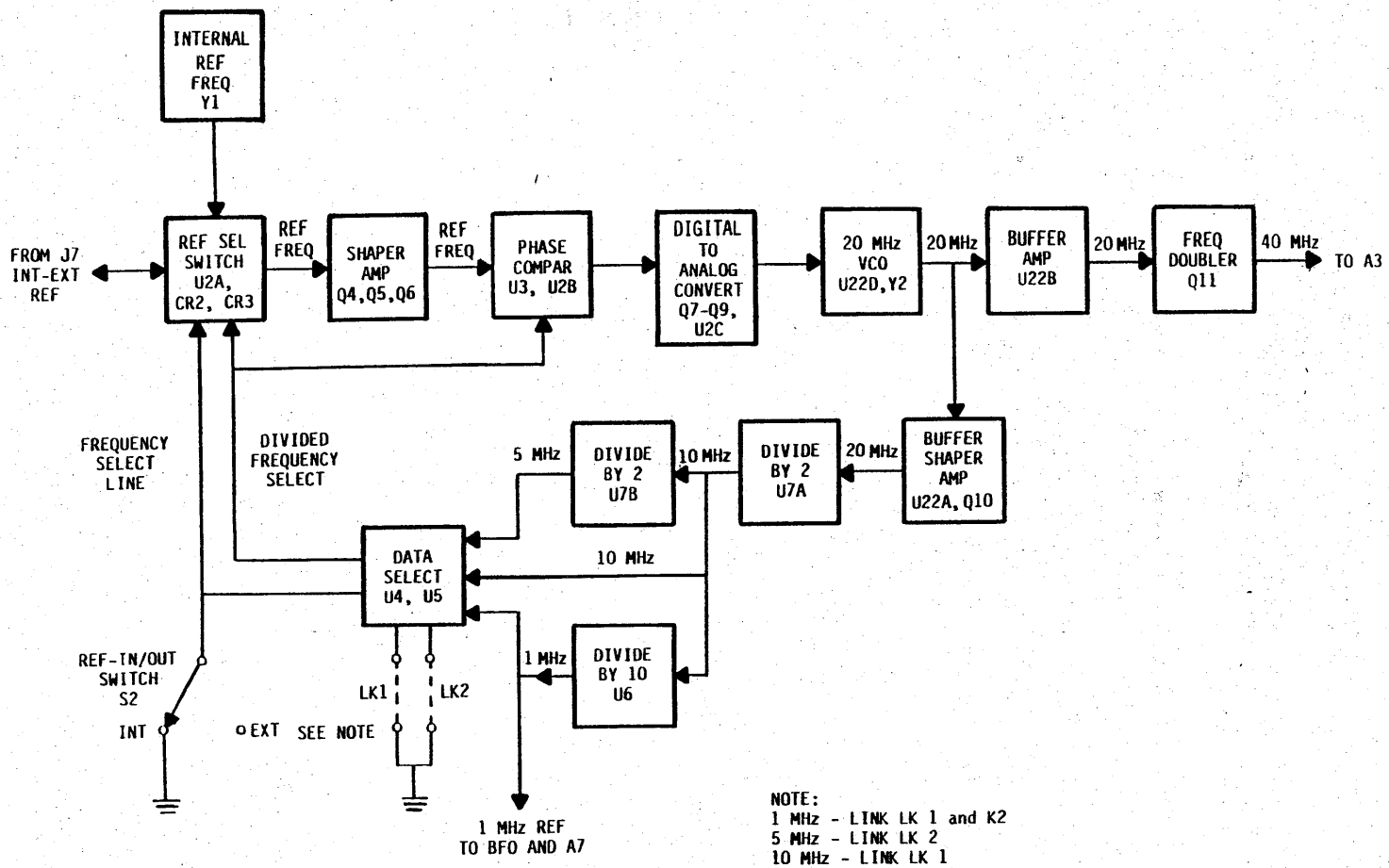
signal through a TTL square wave shaper Q6 to one clock input of the phase comparator. (See Paragraph 4.3.10.4, item 3.) The 20 MHz voltage controlled oscillator, described in Paragraph 4.3.10.4, item 2, is stabilized through the use of this reference frequency. The 20 MHz output of the oscillator is divided by three dividers (two - 2, U7A and U7B and a -10, U6). The two dividers (- 2) are contained in a single dual D flip-flop. The clock signal (20 MHz) is applied to the clock input of U7A. With the $\overline{Q}$ output connected to the D input, the Q output provides the 10 MHz reference. The 10 MHz is also connected to the clock input of the second flip-flop and to the divide by 10 circuit. The second flip-flop Q output provides the 5 MHz reference signal. The divide by 10 circuit is a two stage divider (- 2 and - 5). The 10 MHz drives the clock input for the divider by 5 and B input pin 1. The output of this divider (QD pin 11) is connected back to the clock of the second (- 2) at A input pin 14. Dividing by 5 first then by 2 provides a more symmetrical 1 MHz reference. The 1 MHz signal is output from the divider (- 2) at QA output pin 12. The 1 MHz, 5 MHz and 10 MHz frequencies derived from these dividers are available for reference through data select switches U4 and U5. The 1 MHz reference is routed directly to the BFO synthesizer and to the first local oscillator synthesizer through NAND gate U11C and connector J2. One of the three frequencies will be selected by data select U5 and routed to rear panel connector J7. Either one of the three frequencies may be selected by proper connection of links LK1 and LK2. In this internal mode, data select C of both U4 and U5 is held low through the INT/EXT switch. Linking LK1 makes data select A low which outputs D0 input of both U4 and U5 to their respective Y outputs. For U4 this is 5 MHz, for U5 it is 1 MHz. When only LK2 is linked data select A will be high and B low which connects both D1 inputs to the Y outputs of both (U4-5 MHz, U5-1 MHz). When LK1 and LK2 are linked data select A and B are held low which outputs D3 of both U4 and U5 (U4-5 MHz, U5-10 MHz). As noted in this internal mode, U4 always selects the 5 MHz. It is then routed to the phase comparator as the oscillator reference signal. The output frequency selected by U5 is routed through resistor R13 to buffer amplifier stages Q2 and Q3. These stages provide for output into 50 ohms through a high pass filter, L1, C6 and C7, and connector J7 on the rear panel. The high pass filter also provides filtering for reference frequencies applied externally through J7 while resistors R8 and R9 provide a 50 ohm impedance to the incoming reference frequency.

4.3.10.3 External Mode

In this mode of operation the INT/EXT switch is set to EXT and this line goes high from the +5 volts through resistor R78. This causes transistor Q1 to turn voltage regulator U1 off which in turn turns off the internal crystal oscillator Y1. When an external oscillator is connected to connector J7 on the rear panel, the input is routed through the high pass filter, and capacitor C8 to the base of transistor switch Q4. The input of NOR gate U2A is now high which in turn keeps the base of Q5 low through diode CR3. Transistor Q4, whose base is no longer low, conducts which applies the external reference through the TTL shaper to the same clock input of the phase comparator that the 5 MHz reference was applied in the internal mode. The appropriate reference frequency for application to the second clock input to the phase comparator can be selected through LK1 and LK2 as in the internal mode; however, data select C is now high. Linking LK1 selects D6 (10 MHz), LK2 selects D5 (5 MHz) or both LK1 and LK2 select D4 (1 MHz). The D0, D1 and D2 inputs to U5 cannot be selected when data select C is high (external mode) and no output appears on the Y output of U5.

4.3.10.4 Second Local Oscillator

Figure 4-15 shows a simplified functional block diagram of the second local oscillator. The circuit consists mainly of a crystal referenced, voltage controlled oscillator, a frequency doubler output circuit and a phase lock loop includes amplifiers, an ECL to TTL buffer, three frequency dividers (two - 2 and - 10), reference frequency select circuit, a phase comparator and a digital to analog converter. The three dividers are used to provide a choice of reference frequencies for internal or external reference.



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 4-15. Second Local Oscillator Functional Block Diagram

1. Phase Lock Loop. The 20 MHz oscillator frequency is kept on frequency through a phase locked loop (See Figure 4-11). The oscillator output is routed through a divide by N circuit that provides as oscillator reference frequency. This divided oscillator frequency is coupled to the second clock input of a phase comparator. The phase comparator, described below, detects any phase shift between the oscillator frequency and a reference frequency also connected to the phase comparator. The phase comparator then changes the digital-to-analog converter output voltage which is connected to the oscillator varactor and cyrstal. This then causes the oscillator frequency to change. This loop action will continue until the oscillator frequency is brought into phase (same frequency) with the reference frequency.

2. Voltage Controlled Oscillator. The 20 MHz oscillator consists of an ECL OR gate U22D, 20 MHz crystal Y2, varactor CR4, resistors R47, R48, R49 and R50 and capacitors C34 through C38. Oscillation frequency is derived from the parallel combination of crystal Y2 in series with C37 and with varactor CR4 in series with C34. The dc voltage applied at the junction of CR4 and Y2 controls the reactance of the parallel circuit, mainly through CR4. This dc voltage, controlled through the phase lock loop described in Paragraph (1) compensates for any frequency shift of the oscillator. The oscillator output is coupled to two buffer amplifiers U22A and U22B. Buffer U22A is used to drive a TTL shaper buffer amplifier, Q10, which shapes the oscillator output into a square wave for input to the divider. These circuits are described in Paragraph 4.3.10.2 and 4.3.10.3. Buffer U22B drives a frequency doubler circuit, Q11, and associated components. This tuned circuit selects the 40 MHz component of the signal and outputs it through J3 to circuit card A3 as the second oscillator frequency.

3. Phase Comparator and Digital-to-Analog Converter. The phase comparator is used to detect the phase shift between the reference frequency and the oscillator frequency and to apply control to the digital-to-analog converter in relation to that phase shift. The comparator consists of dual flip-flop U3A and U3B and NAND gate U2B. Flip-flop U3A is clocked from the reference frequency while U3B is clocked from the divided oscillator frequency. The D inputs to both flip-flops are held high through the +5 volts. When both Q outputs are high the output of NAND gate U2B goes low, resetting both flip flops with a delay through R32 and C20. Thus when the positive edge of a clock signal clocks a flip-flop, Q goes high while $\overline{Q}$ goes low. If the two clock signals to the flip-flops are in phase, the $\overline{Q}$ outputs then will go high from the reset action through NAND gate U2B, initiated from the leading edge of both clock pulses. The $\overline{Q}$ outputs will remain high through the on-off period of that particular clock pulse. Except for a small delay time introduced by the flip-flops the $\overline{Q}$ outputs will be high most of the time when the two clock signals are in phase. (See Figure 4-16). When the oscillator frequency leads the reference signal (frequency high), the $\overline{Q}$ output of U3B remains on less than the $\overline{Q}$ output of U3A because the leading pulse sets back to Q on U3B before the lagging pulse of the reference signal sets back to Q on U3A. The reverse of this is true when the oscillator frequency lags the reference signal (frequency low). The two $\overline{Q}$ outputs of the phase comparator are coupled to a digital-to-analog converter which consists of transistors Q7, Q8 and Q9, resistors R33 through R39 and capacitors C24 through C26. The $\overline{Q}$ output of reference flip-flop U3A is connected to the emitter of Q7 through R33 while the $\overline{Q}$ output of the oscillator flip-flop U3B is connected to the emitter of Q9 through R34. When the oscillator and reference signal are in phase, the two outputs are the same and transistors Q7 and Q9 conduct at a rate dependent on the amplitude and time period of the pulse. With the amplitude always constant, the amount of conduction then depends only on the time period. When the pulse goes the emitters of Q7 and Q9 go more positive causing them to conduct less and when the pulse goes low, they conduct more. The voltage output at the common collectors of Q8 and Q9 would tend to follow this rise and fall in the pulse; however, the inverted signal at the base of Q8 also causes it to conduct less when the pulse is high and more when the pulse goes low. This

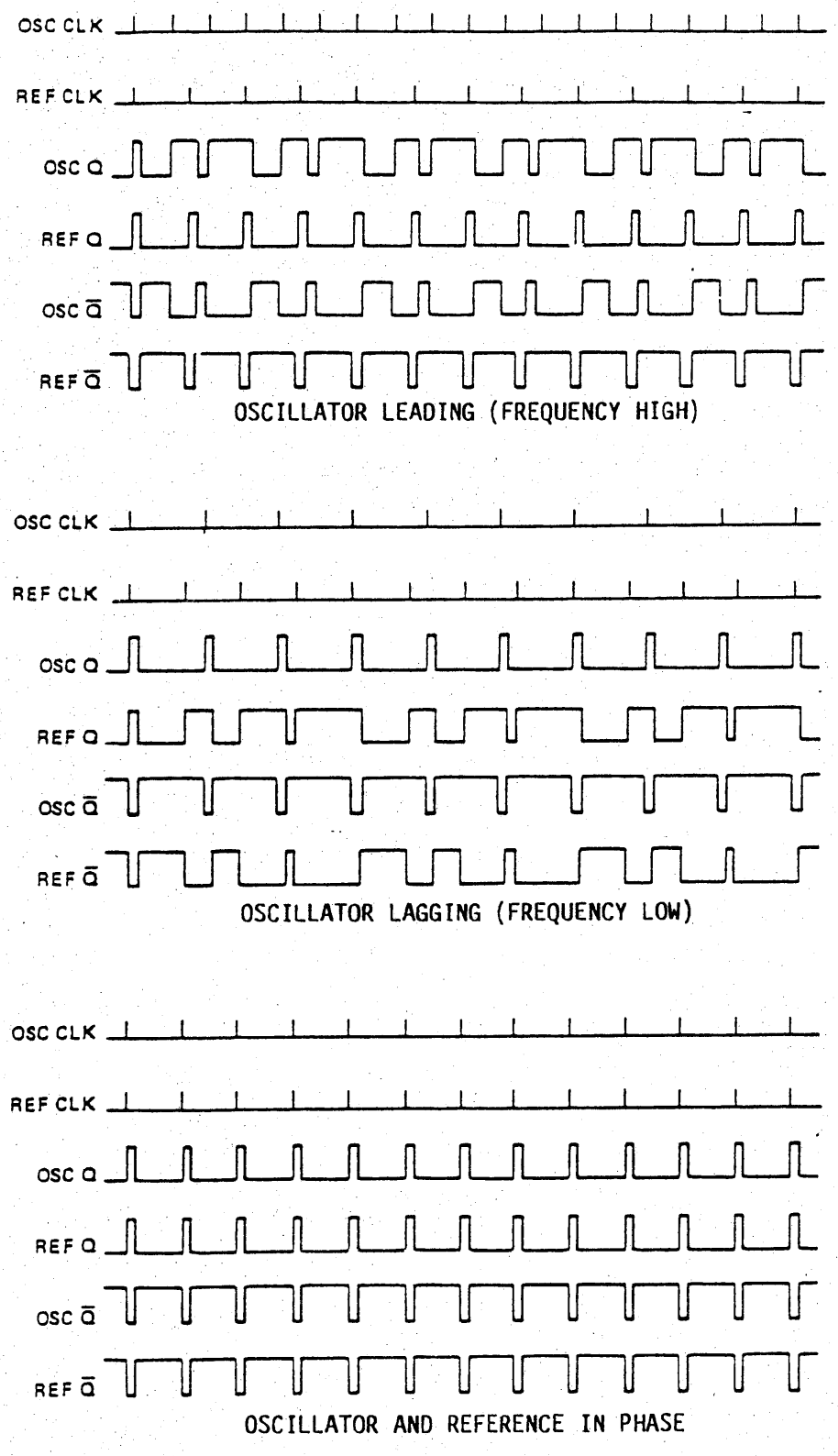


Figure 4-16. Waveform Diagram: Phase Comparator

action converts the pulse; however, the inverted signal at the base of Q8 also causes it to conduct less when the pulse is high and more when the pulse goes low. This action converts the pulse signals into a dc level sawtooth waveform at the Q8-Q9 common collectors. The lowpass filter, C25, C26 and R39 smooths this waveform and dampens sudden changes caused from changes in the phase comparator pulse rates and in turn stabilizes the phase lock loop. When oscillator frequency increases, the pulse rate increases at Q7 and decreases at Q9, causing a reduction of the dc level output. When oscillator frequency decreases the reverse action takes place. This analog dc output is coupled through R47 to the oscillator for frequency control.

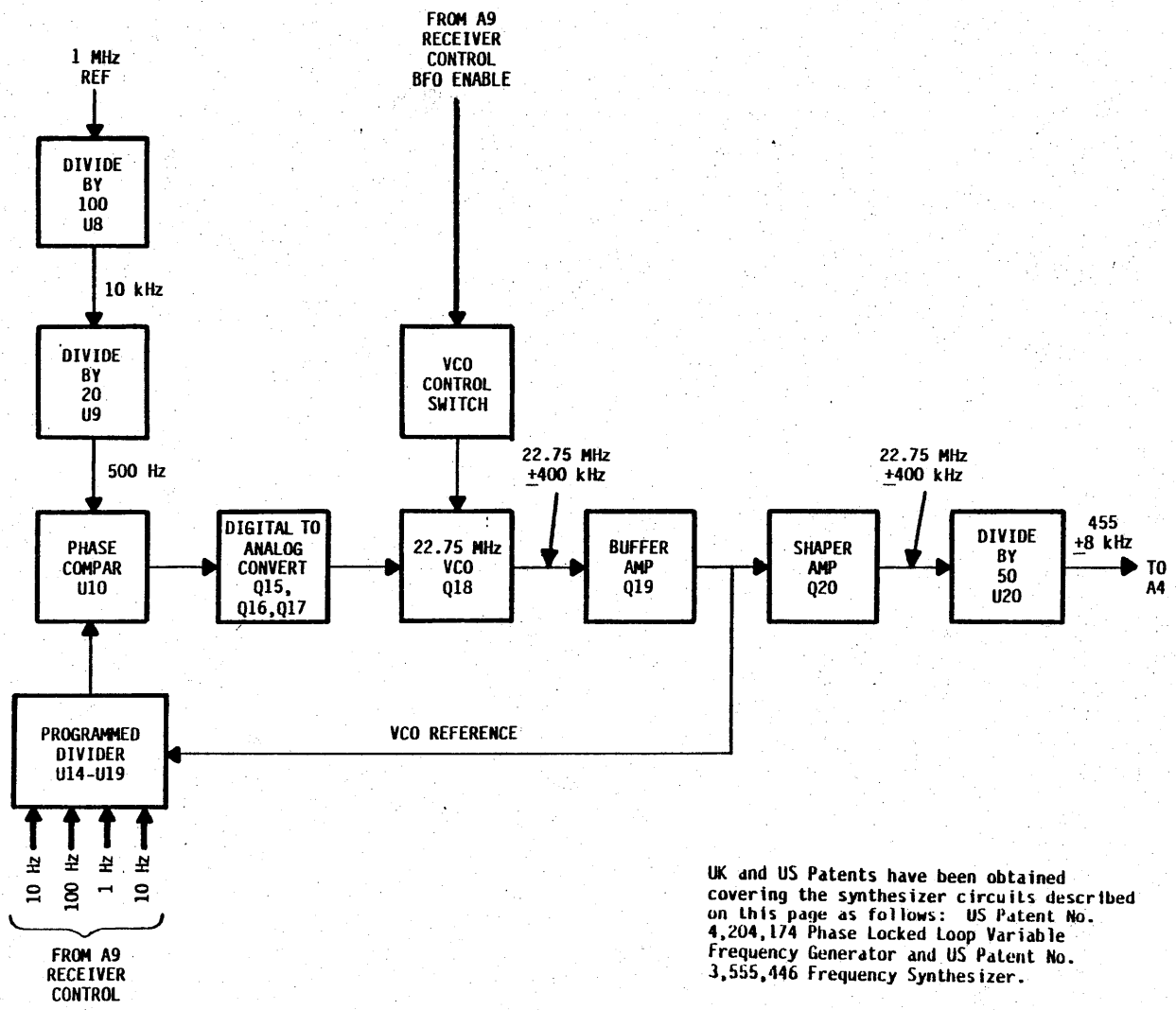
4. Out of Lock Detector. The out of lock (OOL) detector consists of NAND gate U2C, resistors R43 and R44 and capacitors C29 and C31. The NAND gate output is held low (Phase loop in lock) by the $\bar{Q}$ outputs of the phase comparator. The resistor capacitor combinations R43-C29 and R44-C31 integrate the square wave signal to provide a constant high on the two NAND gate inputs. If either or both of the two Q outputs from the phase comparator remains low the output of the NAND gate will go high. The OOL output from this circuit is routed to A9 front panel control for processing.

4.3.10.5 Beat Frequency Oscillator (BFO)

Figure 4-17 is a simplied block diagram of the beat frequency oscillator. This circuit provides the variable 455 kHz BFO for Receiver CW and sideband operation. The BFO is varied plus or minus 8 kHz through receiver control. The oscillator operates in a phase locked loop which consists of a voltage controlled oscillator (VCO), a buffer amplifier, a programmed divider, a phase comparator and a digital-to-analog converter. A divide by 2000 circuit is included to provide a 500 Hz reference signal for the phase comparator. The VCO operates at a center frequency of 22.75 MHz which is 50 times the BFO center frequency or 455 kHz. The oscillator output is routed through a buffer amplifier. TTL shaper, divide by 50 circuit and filter to provide the 455 kHz BFO to the A4 circuit card. An out-of-lock (OOL) circuit is also included to detect any out of lock condition of the phase lock loop.

1. Phase Lock Loop. The phase lock loop for the BFO oscillator functions in the same way as the circuit described for the second local oscillator except the divide by N is made variable through BFO input data to the divide by N circuit.

2. Voltage Controlled Oscillator. The VCO consists of field effect transistor Q18 opto-isolator U21, coils L4 and L5, resistors R66 and R67, capacitors C52 through C56 and C59 and varactors CR6 and CR7. The capacitive reactance of the two varactors in conjunctions with L4 determines the frequency at which the circuit will oscillate. Since varactors change capacitance in relation to the level of the dc voltage applied, the frequency of the oscillator is controlled from the output of the digital-to-analog converter that is applied to varactors CR6 and CR7 through coil L3. Opto-isolator U21, connected to the source of Q18 through resitor R67, provides for on-off control of the oscillator by isolated control of the oscillator source bias. When BFO is enabled in the CW and sideband modes, U21 is enabled through pin 2 which in turn completes the bias path for Q18 through R67. The output of the oscillator is coupled through capacitor C57 to the gate of field effect transistor Q19 which acts as a buffer amplifier between the oscillator and two output circuits. One output of the buffer amplifier provides the oscillator reference frequency through capacitor C72 to the progammed dividers. This circuit is described in Paragraph 3. The second output is coupled through capacitor C60 to a shaper circuit, Q20, R72, R73, R74 and C61. This circuit shapes the waveform into a square-wave for the TTL logic of the divide by circuit U20. The dual decade counter U20 is externally strapped to provide a division of 50 on its QD output, pin 9. The variable 22.35 to 23.15 MHz oscillator signal is



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 4-17. BFO Functional Block Diagram

reduced in frequency by the division of 50 which provides the 447 to 463 kHz BFO. This output is filtered through the filter network consisting of C63, C64, C65, L6, R75, R76 and R77. This filter shapes the digital waveform from U20 into an approximate sine wave signal before being routed to circuit card A4 through connector J4.

3. Programmed Dividers. The programmed dividers determine the divide-by-N number by which the oscillator frequency will be divided for a variable reference to the phase comparator. The program dividers consist of presettable BCD decade counters U14 through U18, divide by 10 or 11 2-modulus controller U19, NOR gates U12A through U12D and AND gates U13A through U13C. The program divider has two reference inputs: the oscillator frequency coupled through C72 to the V reference and clock inputs of U19 at pins 15 and 16 and the BFO data control inputs to U15 through U18. It is the BFO data inputs in conjunction with U19 that sets the divide by N number for dividing the VCO frequency. To divide the 22.75 MHz to 500 Hz, for the second clock input to the phase comparator, would require a division of 45500. The five decade counters are externally strapped to count down from a maximum count of 100000 (99999 + 1). The actual data then that would be set on the BFO inputs would be 100000 - 45500 = 54500; however due to gating restrictions between the decade counters the actual number set at the BCD inputs is 54509 at center frequency (455 kHz). The BFO is adjustable plus or minus 8 kHz so that the swing in the BCD inputs must be from 53709 (54509 - 800) to 55309 (54509 + 800) with 54509 as center. At center frequency counter U18 receives the 10 Hz BCD digits on its parallel inputs P0 through P3 with P0 and P3 ($2^0 + 2^4 = 9$) high. Counter U17 receives the 100 Hz digits with all input low (0), U16 receives the 1 kHz digits with P0 and P2 ($2^0 + 2^2 = 5$) high, and U15 receives the 10 kHz digits with only P2 ($2^2 = 4$) high. Counter U14 is strapped P0 and P2 ($2^0 + 2^2 = 5$) to the +5 volts (high) and P1 and P3 to ground (low). This supplies the 100 kHz digit which is always 5. Counter U15 receives only the 2^0, 2^1 and 2^2 BCD digits since the 10 kHz swing is never greater than 7. The counter is a two modulus divide by 10 or 11 controller and will divide by 10 or 11 for different periods in the clock signal. The TC output pin 15 of U18 coupled to the M1-M2 inputs of U19 determine the periods at which it will divide with either 10 or 11. NOR gate U12C ensures that the count enable input of U18 goes low when TC goes high. This assures that the TC output will be retained long enough for action on the M1-M2 inputs of U19. The QTTL output (pin 11) is used to clock the decade counters U14 through U18 and as a reclocking source for NOR gate U12A. Four control inputs, parallel enable (PE), count enable parallel (CEP), count enable trickle (CET) and reset (R) select the counters mode of operation. The R and CET of all counters is held high through the +5 volts connected to all counter CET and R inputs. The CEP input of counter U17 (100 Hz) is also held high from the same +5 volts since this counter does not receive a carry out from previous counters. The CEP of counter U16 is high only when the TC output of U17 is high, the CEP of U15 is high only when the TC output of both C16 and C17 through AND gate U13A are high and the CEP input of U14 is high only when the TC output of both U15 and U16 through AND gate U13B are high. This AND gating of the TC outputs help prevent extra pulses from occurring that are caused from delays in the counters. The PE of all counters are alternately low and high as the TC outputs to inverter U12B is alternately high and low. With the R and CET of all counters held high (counter resets when R is low) the count mode is enabled when CEP and PE goes high. When PE goes low the counters will synchronously load the data from the BFO inputs into the counters with the count occurring each 500 Hz. The counters output on TC only when PE is held high; however when CEP is held low the TC output will be retained until the next clock pulse. The TC output of the programmed dividers is connected to one input of a two input NOR gate U12A. The clock signal is connected the second input so that any unwanted pulses, created by delay in the counters and not in sequence with the clock pulse, will be rejected. The output of U12A is routed through inverter U12D to one clock input of the phase comparator as the oscillator reference frequency.

4. Reference Frequency. The 1 MHz reference frequency supplied from internal/external reference circuits is divided by 2000 to provide a 500 Hz reference

frequency to the phase comparator. This division of 2000 is accomplished with two dual decade counters U8 and U9. Counter U8 provides a division by 100 while counter U9 provides division by 20. Each counter has two divide by 2 circuits and two divide by 5 circuits and are externally strapped to provide the division by 100 and 20. The division by 100 is accomplished by using all four dividers in the order shown (- 2 = 500 kHz, - 5 = 100 kHz, - 5 = 20 kHz and - 2 = 10 kHz). The divide by 20 is accomplished in the same manner except its input is the 10 kHz output of the - 100 and the second - 5 is bypassed (- 2 = 5 kHz, - 2 = 500 Hz). The resultant 500 Hz output is coupled to the clock input of D flip-flop U10A. This flip-flop is contained in a dual flip-flop package which together with NOR gate U11A make up the phase comparator.

5. Phase Comparator and Digital-to-Analog Converter. As described previously, the 500 Hz reference frequency is connected to flip-flop U10A. The second flip-flop U10B receives its clock signal from the programmed dividers. The D inputs of both flip-flops are tied to the +5 volts (logic 1) while both Q outputs are connected through 2 input AND gate U11A and resistor R83 to the reset of both flip-flops. Both flip-flops will reset each time that both Q's go high, causing a logic 0 at the resets of both flip-flops. The clock input signal to the U10A (reference) consists of positive going pulses while the signal from the programmed divider (oscillator reference) also contains positive going pulses and is connected to the clock input of U10B. Each flip-flop triggers Q on (high) the positive going pulse of its respective clock signal and at the same time triggers $\overline{Q}$ to zero (low). Previously as described, when both Q outputs are high the output from AND gate U11A is low clearing both flip-flops through R83. This resets the Q outputs to low and the $\overline{Q}$ outputs to high. Refer to Figure 4-16. The two Q outputs are connected to the digital to analog converter which consists of transistor Q15, Q16 and Q17 and their associated components. This circuit operates in the same manner as the digital to analog converter described in Paragraph 4.3.10.4 (3) except that adjustments in the BFO frequency provide a different setting of the dc control voltage. This causes the VCO to change frequency in relation to the BFO setting.

6. Out of Lock Detector. The out of lock detector consists of NAND gate U11D, resistors R57, R58 and R84 and capacitors C83 and C86. This circuit operates in the same manner as the second local oscillator OOL circuit.

4.3.11 Front Panel, A9A1

Refer to Figure 4-18, Front Panel Block Diagram, as an aid in understanding the following description. The Front Panel contains Keypad Switches, Switch Demultiplexer, two LCD's and Audio/IF Gain Controls.

4.3.11.1 Keypad Switches/Switch Demultiplexer

Two sets of switches, containing a total of 40 keypads, are used to enter receiver control data from the front panel. Each pushbutton switch is SPST-NO, connected to one of the eight inputs of an addressible multiplexer. Depressing any switch brings its input from high to low.

Each of the five Demultiplexers are enabled by the I/O Read signal from the CPU. Each encoder is addressed from 0 to 7 by the ICOO-ICO2 address lines. Demultiplexer outputs, representing which switch, 0-7, on each demultiplexer was depressed, are read out on the LDB0-LDB4 bits of the 8-bit buffered data bus. The CPU performs switch scanning every 25 ms under program control.

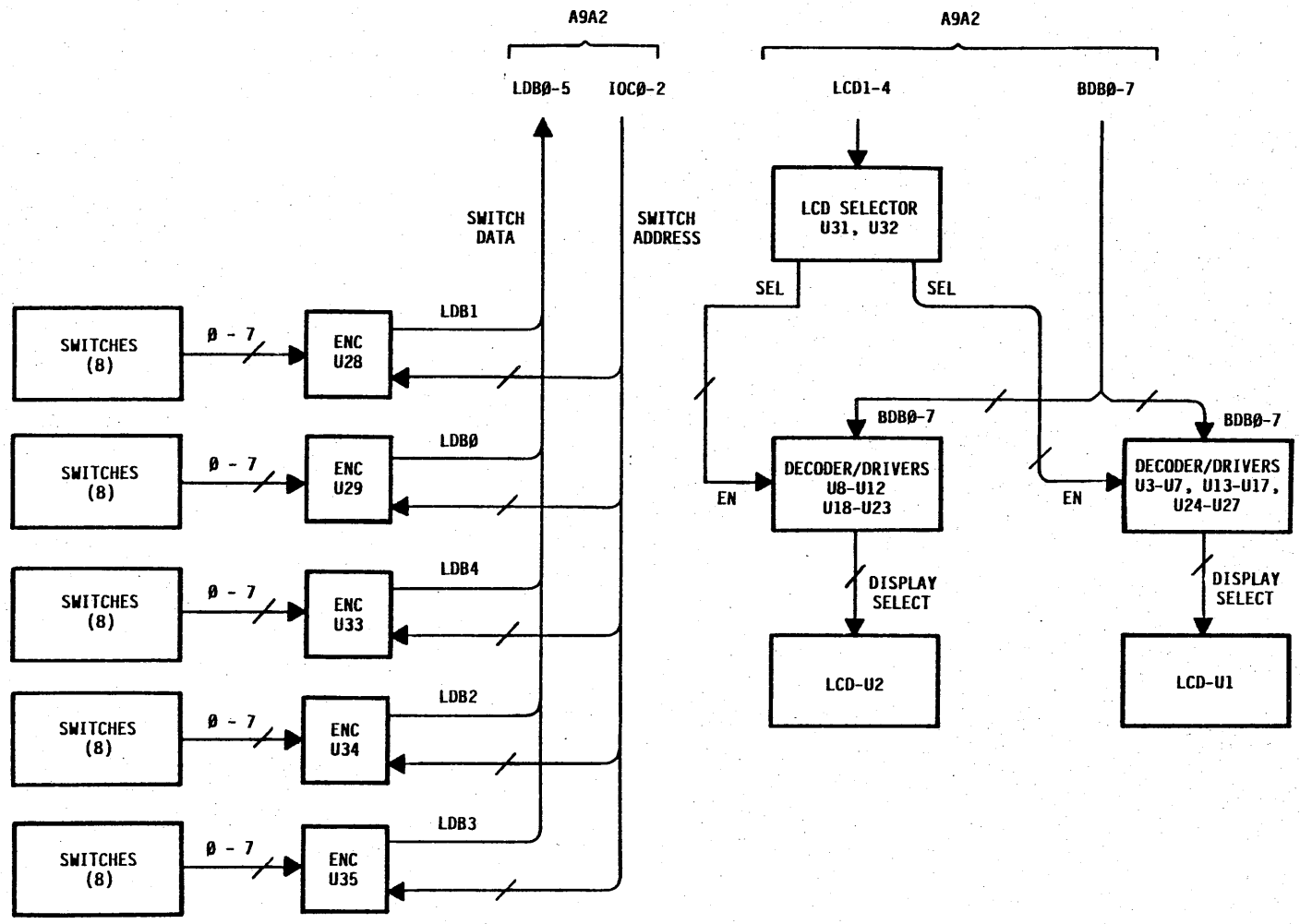


Figure 4-18. Front Panel, A9A1, Block Diagram

4.3.11.2 LCD's

Two LCD's are contained on the front panel for displaying receiver status. Receiver and BFO frequency are displayed on U1, while detection mode, gain mode, tuning mode, remote/local, bandwidth and metering are displayed on U2. The 8-bit buffered data bus directly drives ten 4-line LCD drivers and thirteen BCD to 7 segment decoder/drivers for the numerical displays. Multivibrator U30 provides 100 Hz to drive the two LCD's at the proper refresh frequency.

Timing to the LCD drivers is provided by strobe signals from BCD-decimal decoder U32. Timing to the 7-segment drivers is provided by strobe signals from 4-bit latch/decoder U31. These two decoders are driven from the LCD0-LCD4 signals generated on A9A2. When a strobe signal, in program sequence, enables a LCD driver or a 7-segment driver, the data at its input port is latched into the driver.

4.3.11.3 Audio/IF Gain Controls

Audio and IF gain controls are contained on the front panel for control of these functions. Control and audio signals connecting with these components are routed through the A9A2 circuit card to the A4 Main IF/AF card, with no connection to the digital circuitry on A9A2. A complete description of these components is found in paragraph 4.3.4.

4.3.12 Receiver Control, A9A2

Refer to Figure 4-19, Receiver Control Block Diagram, as an aid in understanding the following description. The Receiver Control consists of a CPU Data Buffer, CPU Address Decoders, Front Panel Switch Buffer, Secondary Address Counter, 1st LO Tuning Data Buffer, BFO Tuning Data Buffer, Main IF/AF Control Bus, Status Latch and the Out of Lock (OOL) Latch. The receiver control interconnects the receiver circuits and front panel to the buffered data bus which is controlled by the Microcomputer, A6A2. This enables the Microcomputer to direct and monitor the activities of the receiver circuits.

4.3.12.1 CPU Data Buffer

Data flow between A9A2 and A6A2 is via the 8-bit bidirectional bus, IOD0-IOD7. Data flow is buffered and controlled by U1, U2 and U13. The bidirectional switches U1 and U2 are configured to transfer data from A9A2 to A6A2 during a READ cycle. The tri-state, 8-bit latch, U13, is used to transfer data from A6A2 to A9A2 during a WRITE cycle. Address inputs, IOC0-IOC3, from the Microcomputer are used to generate strobe signals to control data transfer through the buffer.

4.3.12.2 CPU Address Decoders

Address inputs IC00-IC03 from the Microcomputer are decoded by U14 and used to generate strobe signals for operation of the remainder of A9A2. U14 is timed through the WSTB signal to the strobe input of U14, and also by multivibrator U3. The U14 strobe outputs are latched in proper timed sequence and are used to control data flow to various receiver control functions.

Address inputs IC00-IC03 are also decoded by secondary address decoder U6 in conjunction with one of the strobe outputs from U14. These secondary strobe outputs are used to control the status and OOL latches.

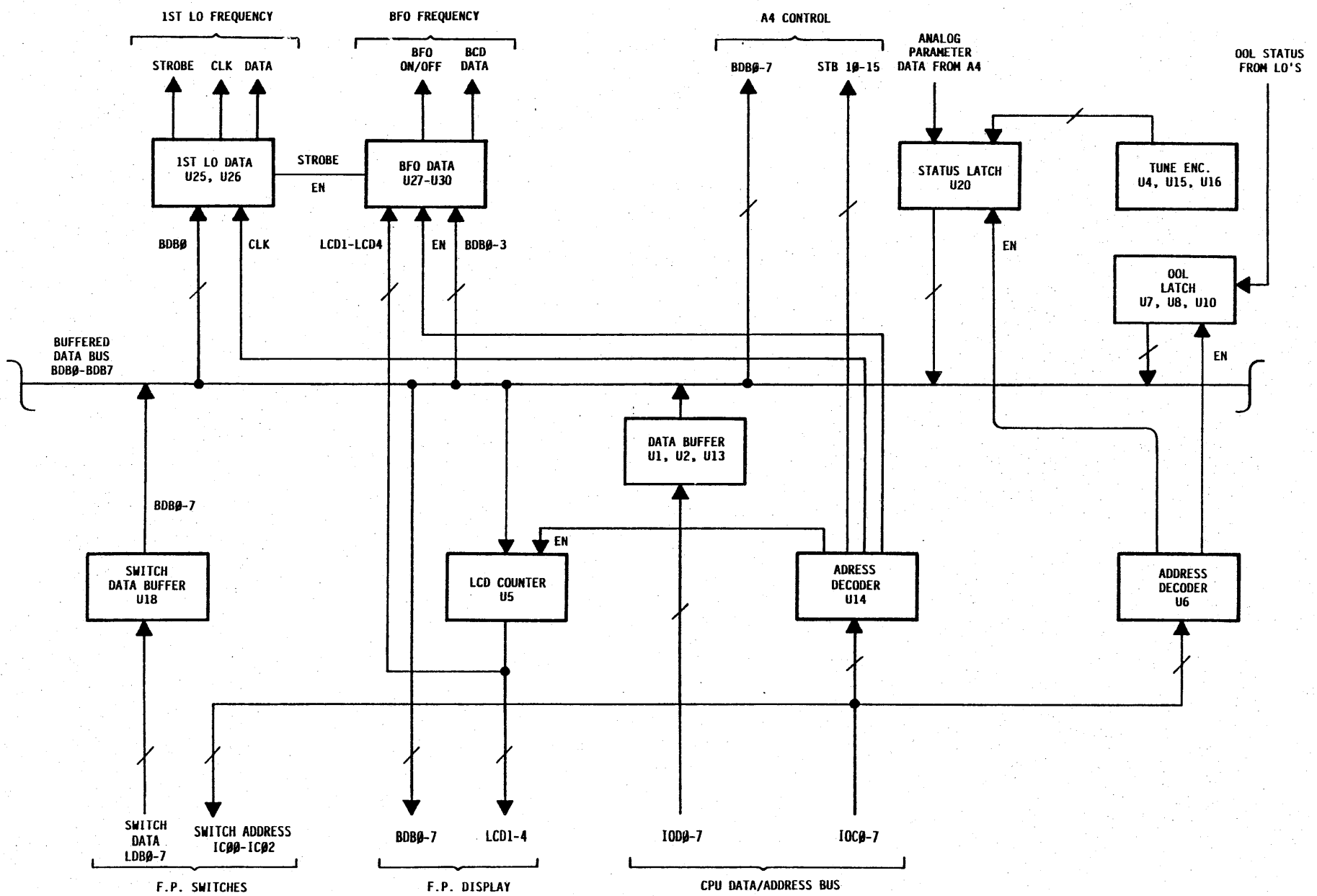


Figure 4-19. Receiver Control, A9, Block Diagram

4.3.12.3 Front Panel Switch Buffer

Switch address data, IC00-IC02, is sent to the front panel and selectively scans the switch demultiplexer. The outputs of the switch demultiplexer, LDB0-LDB7, is sent to the front panel switch buffer, U18. The output of U18 is selectively transferred to the buffered data bus by the I/O Read control signal from the Microcomputer.

4.3.12.4 Secondary Address Counter

The Secondary Address Counter, U5, generates the secondary address select signals which select the front panel display decoders and latches. The LCD1-LCD4 signals are transferred from the buffered data bus when properly enabled by a U14 strobe output.

4.3.12.5 1st LO Tuning Data Buffer

Processed receiver frequency data from the microprocessor is routed through data line BDB0 to data buffer U25, 26. The frequency data, properly timed by U14 strobe outputs, is serially routed through U26A to the 1st LO, A7. Strobe output from U14 is routed through U26B as a clock signal to A7. The Q_0 output from BFO buffer U30 is routed through U25A as a strobe signal to A7.

4.3.12.6 BFO Tuning Data Buffer

Processed BFO frequency data is routed through data lines BDB0-BDB3 to latches U27-U30. Three outputs of the secondary address counter U5, drive the binary inputs of four 8-bit addressible latches U27-U30. These latches supply in the BCD tuning data to the programmable divider on the BFO, A8. Timing for the latches is supplied by a U14 strobe output. The Q4 output of U27 supplies a BFO enable signal through Q2.

4.3.12.7 Main IF/AF Control Bus

Data lines BDB0-BDB7 and U14 strobe signals STB10-STB15 are routed to the Main IF/AF card, A4. These signals will be latched through the IF/AF control logic to select bandwidth, AGC mode and audio matrix routing.

4.3.12.8 Status Latch

The main RF, ISB RF, IF Gain and AF comparator circuits from A4 are connected to four inputs of status latch U20. The inputs are strapped to +5 V through pull up resistors. The actual input levels to U20 will be 0 or +5 V, depending on the status of the A4 comparators. U20 is strobed by U6 to transfer the four comparator inputs to BDB0-BDB3 on the data bus for reading by the microcomputer.

The optical encoder, U4, U15 and U16, is driven from the front panel tune wheel. The outputs of the encoder drive the remaining two inputs of status latch U20. Two streams of clock pulses are transferred to BDB4 and BDB5 when the tuning wheel is rotated.

4.3.12.9 OOL Latch

The out of lock circuit monitors the condition of the three phase lock loops, drives OOL indicators on A9 and supplies OOL data to the buffered data bus. The OOL signals are latched through flip-flops U8 and U10 by a U6 strobe output. These latched outputs drive fault indicators DS1-DS4 through U11 and U12. The flip-flop latched outputs are also connected to the inputs of latch U7 which is also timed by a U6 strobe output. The latch, in

program sequence, outputs the status of the OOL circuits to the buffered data bus which is then routed to the microcomputer. The processed FAULT data from the microcomputer is routed through the secondary address counter, U5, to latch U30. The U30, Q5 output drives the front panel fault indicator through U22B.

4.3.13 Power Supply, A10

Refer to schematic diagram, Figure 7-15. The module operates from an ac line input, steps down the voltage, rectifies the ac, filters and regulates the various divided voltages. The unit contains a circuit card switch which provides for switching the transformer input for 100, 120, 220 or 240 volts ±10% operation from the input power line. This line frequency must be between 48 and 420 Hz. AC input power is applied to the receiver through the POWER-ON toggle switch located on the front panel. The input power is also fused through F1, located on the rear panel for easy access. The 100 or 120 volt input must be fuse differently than the 220 or 240 volt input. The alternate fuse is contained in a fuse holder located inside the power supply.

4.3.13.1 DC Power Output

The secondary of transformer T1 contains three separate windings that provide the six different dc outputs for receiver operation. These six dc outputs, along with their tolerances are listed below:

+20 ±1 volt
+15 ±0.5 volt
+15 volts unregulated (nominally +22 volts)
-15 ±0.5 volt
+5 ±0.5 -0.2 volts
+5 volts unregulated (nominally +10 volts)

Conventional bridge rectifiers CR1, CR2 and CR3 provide ac to dc rectification while capacitors C1, C4, C7 and C10 provide filtering and smooth the pulsating dc. Capacitors C1 through C9 are connected adjacent to the three voltage regulators to suppress possible oscillations. The rectified and filtered dc from one winding, 12 to 13, of the transformer is coupled to dc regulator A10A2, which provides the regulated +20 volts to pins 1 and 14 of A10J3. Winding 6 to 8 provides the +15 volts unregulated to pins 3 and 16, the +15 volts regulated through regulator U2 to pins 7, 8, 10, 11 and 24 and the -15 volts regulated through regulator U3 to pins 22 and 23. Winding 9 to 11 provides the +5 volts unregulated to pins 5 and 18 and the +5 volts regulated through regulator U1 to pins 2, 4, 15 and 17 of A10J3. The six dc outputs from A10J3 are routed to various applications throughout the receiver circuitry.

SECTION V
MAINTENANCE

5.1 GENERAL

This section provides detailed procedures for conducting preventive maintenance, performance testing, fault isolation, and corrective maintenance on the RA6793A HF Receiver. The maintenance areas covered by these procedures include: inspection for damage and wear, cleaning and lubrication, performance tests, operational checkout and fault isolation, board level fault isolation, and receiver assembly and disassembly. Performance tests and Built-In Test Equipment (BITE) checkout procedures are presented in sufficient detail to allow fault isolation to the individual module/printed circuit board. Routine application of preventive maintenance and performance test procedures will provide extended Receiver life, early indications of potential operating problems, and optimum Receiver performance. A recommended Preventive Maintenance Schedule is shown in Table 5-1.

Table 5-1. Preventive Maintenance Schedule

PROCEDURE	INTERVAL	COMMENTS
Inspection for Damage or Wear	60 days	Interval variable depending on operating environment.
Cleaning	30 days	Interval variable depending on equipment use.
Lubrication	None	None
Performance Tests	180 days	Interval variable depending on location/application requirements.

5.2 PREVENTIVE MAINTENANCE

The following paragraphs detail the preventive maintenance procedures to be used when servicing the RA6793A HF Receiver.

5.2.1 Inspection for Damage or Wear

Many potential or existing faults can be detected by making a visual inspection of the unit. For this reason, a complete visual inspection should be made on a routine basis and whenever the receiver is inoperative. At a minimum, the following items should be visually inspected.

1. Inspect the equipment covers and front panel for condition of finish and panel marking.
2. Inspect for dents, punctures, or warped areas.
3. Inspect quarter-turn fasteners and receptacles.
4. Inspect the external surfaces for loose or missing screws or washers.
5. Inspect the receptacles for condition of pins, contacts, and mounting.
6. Inspect the internal components for signs of deterioration, discoloration, or charring. Check for melted insulation and damaged, cracked, or broken components.

7. Inspect the printed circuit boards for damaged tracks, loose connections, corrosions, or other signs of deterioration.
8. Insepct the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

5.2.2. Cleaning and Lubrication

Cleaning

Cleaning should be performed to remove accumulated dust, grease, and other contamination, and to ensure trouble-free operation.

CAUTION

Avoid the use of chemical cleaning agents containing benzene, toluene, zylene, acetone, or similar solvents. These chemicals may damage the plastics used in this receiver.

1. Exterior - Dust the cabinet off with a soft cloth. Dust the front panel controls with a small-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean, lint-free cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the front panel.

2. Interior - Dust in the interior of the unit should be removed before it builds up enough to cause arcing and short circuits during periods of high humidity. Dust is best removed by dry, low-pressure air. Dirt clinging to surfaces may be removed with a soft-bristled paint brush or a clean, lint-free cloth dampened with a mild detergent and water solution. Use a cotton-tipped applicator for cleaning in narrow spaces and on the circuit boards.

3. Switch Contacts - When maintenance is necessary due to accumulated dirt and dust on the contacts, observe the following precautions: Clean the switch contacts with isopropyl alcohol or a mild detergent solution. Avoid cleaning solutions containing benzene, acetone, or similar solvents.

WARNING

The filter capacitors used in the power supply will retain an electrical charge after power is removed. The capacitors should be discharged slowly by shorting terminals through a protected resistive device.

Lubrication

Lubrication is unnecessary in the Receiver. If the main tuning shaft appears to be binding during rotation in either direction, perform the following:

1. Disconnct receiver power source.
2. Loosen and remove the tuning knob.
3. Loosen the six (6) quarter-turn fasteners and remove the receiver top and bottom covers.

4. Remove the receiver front panel as directed in Paragraph 5.8.1. Front Panel Assembly.
5. Loosen both tuning-shaft retaininer nuts (one located behind tuning knob, the other located behind tuning-shaft encoding wheel).

CAUTION

Overtightening tuning-shaft retainer nuts may cause damage to tuning assembly and the A9 module.

6. Retighten tuning-shaft retainer nuts finger tight only.
7. Reinstall tuning knob and flywheel and retighten screws.
8. Check for smooth, free operation of tuning knob.
9. Reinstall the receiver front panel as directed in Paragraph 5.8.1. Front Panel Assembly.
10. Reinstall receiver top and bottom covers and retighten six (6) quarter-turn fasteners.
11. Reconnect power source.

5.3 MAINTENANCE SUPPORT EQUIPMENT

Certain procedures involved with both performance testing and board-level fault isolation may require the use of external test equipment to supplement BITE. Table 5-2 lists suggested test equipment by type and required operational characteristics. Not all test equipment listed is required for any one procedure.

Equipment required for a particular test is specified in the procedure for that test.

Table 5-2. Maintenance Support Equipment

INSTRUMENT	SPECIFICATIONS	RECOMMENDED INSTRUMENT OR EQUIVALENT
Digital Voltmeter	Range: 0 to 150 Vac and dc 0 to 1 A ac and dc Display: 3-1/2 digits Accuracy: ±2 L.S. digit	Fluke 8040A-01
Oscilloscope, Dual Trace, Portable AN/USM-425(v)1	Sensitivity: 5 mV/div. Frequency: dc to 100 MHz	Tektronix 465M
RF Millivoltmeter	Range: 300 mV to 3 Vrms Frequency: 100 kHz to 600 MHz Input Impedance: 1M ohm with Accuracy: ±1% of full scale	Boonton 92B
Spectrum Analyzer	Frequency Range: 0 kHz to 110 MHz Frequency Bandwidth: 10 Hz 300 Hz	Hewlett Packard Main Frame HP141T IF Tuning Sec. HP8552A RF Tuning Sec. HP8553B

Table 5-2. Maintenance Support Equipment (Cont.)

INSTRUMENT	SPECIFICATIONS	RECOMMENDED INSTRUMENT OR EQUIVALENT
HI-Impedance Probe, Spectrum Analyzer	Frequency Response: ±0.5 dB from 0.1 to 110 MHz ±3 dB from 1 kHz to 500 MHz Input Impedance: 100k ohms shunt capacity of 3pF@100 MHz with 10:1 divider, 1M ohm with 1 pF@100MHz	Hewlett Packard HP1121A
Distortion Analyzer	Distortion Contribution: 0.1% High Input Impedance Dynamic Range: 80 dB	Hewlett-Packard 334AW/ 0PTH05
SG-1093/ u AM/FM Signal Generator	Frequency Range: 500 kHz to 100 MHz Accuracy: ±0.5% of dial setting Stability: 10 parts in 10^6 Output Level Range: -140 dBm to +20 dBm Modulation: AM -0 to 100% FM ±150 kHz @ 30 MHz Output Impedance: 50 ohms	Hewlett-Packard 8640B 001
Cable Coupler	BNC-SMB	Sealectro 51-075-6801
Junction Box	8 and 600 ohm terminations with test points for J3	Racal A08047
X10 Oscilloscope Probe	Tip Impedance: 10 Megohms, 13.5 pF	Textronix P6105X10
Frequency Counter	Internal Reference Frequency Stability: 1 part per 10^8	Hewlett Packard 5354A
RF Probe	Recommended for use with RF Millivoltmeter	Boonton 91-12F
50 ohm Adapater	Recommended for use with RF Millivoltmeter	Boonton 91-8B
Headphone Set	Minimum: 10 Milliwatts nominal output power into 600 ohm load	Racal/Amplivox V31B

5.4 RA6793A OPERATIONAL CHECKOUT AND FAULT ISOLATION PROCEDURE

Operational checkout of the RA6793A HF Receiver must be approached using a symptom/diagnostic analysis to augment the results of BITE test procedures. Since BITE is not a panacea for all electromechanical problems, a degree of interpretation is necessary by maintenance personnel. The scope of the analysis must include the conditions that preceeded the use of BITE in addition to those during and following its use. Interpretation of the results will, with a probability of greater than 90%, verify the operational readiness

status of the Receiver or isolate a Receiver fault to a specific board. Both verification and fault isolation depend upon careful observation of all symptoms starting with the initial step of energizing the Receiver. Further, for fault isolation, certain assumptions must be made in order to facilitate an intelligent assessment. These assumptions are: (1) the previous configuration of the Receiver is correct, i.e., filter complement installed correctly, system interfaces properly connected; (2) the Receiver was properly installed in an operational position (station); (3) the Receiver was functioning correctly prior to the occurrence of the fault; and (4) all connections, connectors, cables and components had been checked for correct placement, continuity and tightness.

The following procedures detail verification and fault isolation.

5.4.1 Initial Check

1. Verify that the PC wafer in A10J1 on Receiver rear panel matches available line voltage.
2. Energize Receiver by turning POWER ON switch to "ON" position.
3. Observe edge lighting and Liquid Crystal Displays (LCD's). If edge lighting is present and LCD displays contain data, the Power Supply (A10) is working properly. Proceed to step 4.

   IF: a. Edge lighting is not present, the +15 volts from the A10 is malfunctioning. Check this voltage through the A10 and correct the malfunction.

   b. Edge lighting is present, frequency display contains mostly zeroes, and no mode indication is present, either the wafer does not match available line voltage, or the A6A2 Microcomputer Assembly is faulty and should be replaced.

4. Depress the LOCAL/REMOTE pushbutton switch on the front panel. The LCD display should indicate a change in receiver control from no display to REMOTE or vice versa. Repeated pressing of the LOCAL/REMOTE pushbutton switch should alternate the display between no display and REMOTE indications.

   IF: a. The Receiver indicates that it is in the REMOTE mode, and depressing the LOCAL/REMOTE pushbutton does not change the display, either the A6A2 Microcomputer Assembly or the A9 Front Panel Assembly is faulty and must be replaced.

   b. The Receiver display does not indicate that it is in REMOTE, further isolation is possible. Depress the Meter RF/AF pushbutton switch. The meter display should change correspondingly. If it does change, the REMOTE/LOCAL pushbutton switch is probably bad and the A9 Front Panel Assembly should be replaced. If the meter display does not change, initialize the Receiver by depressing the LOCK and AM pushbuttons simultaneously and allow the receiver to initialize (approximately one minute). Once again attempt to change from LOCAL to REMOTE and back; and from RF to AF meter indications. If the display still will not change, the fault is probably on the A6A2 Microcomputer Assembly which should be replaced.

NOTE

Once steps 1 through 4 have been successfully accomplished, it can be assumed with 60% confidence that both the A6A2 Microcomputer and the A9 Front Panel Assemblies are functional. To increase the confidence factor, perform step 5.

5. Ensure that the Receiver is under LOCAL control (indicated by absence of REMOTE in LCD display). Depress the ENTER pushbutton switch momentarily, followed by numerals 12345678. These numerals should appear as 12.345678 on the frequency LCD. If this display is correct, then a confidence factor of 99% can be assumed regarding the total reliability of the A6A2 Assembly and a confidence factor of 60% for the A9 Assembly.

6. Ensure that the Receiver is under LOCAL control. If MAN is displayed in LCD, momentarily depress the MAN pushbutton on the front panel to achieve Manual IF gain control. Once MAN is visible on the LCD, ensure that SHORT, MED, or LONG are not present in the display. If any of these three indications are present, momentarily depress the corresponding SHORT, MED or LONG pushbutton on the front panel to remove the indication from the display.

When set up correctly, only the MAN display should be present in the LCD. Also, ensure that the meter indication is set for RF level. Once this condition has been attained, slowly rotate the IF GAIN potentiometer on the front panel from the full clockwise to full counter-clockwise positions and back again while observing the RF level meter display in the LCD. The RF level display should range from zero (no indication) to full scale and back again to zero. If this range is not attainable, then either the A4 Main IF Assembly (60% probability) or the A9 Front Panel Assembly (40% probability) is at fault and should be replaced.

NOTE

Failure to attain the desired range definitely indicates that proceeding with the BITE checks is useless until the problem is corrected. On the other hand, full range indication demonstrates that the A4 Main IF measurement system used by BITE is functional and BITE checks will yield useful results.

Since steps 1 through 6 are prerequisite to successful BITE testing, BITE may now be effectively applied.

5.4.2 BITE Check

1. Ensure that the initial Check Performance (Paragraph 5.4.1) have been successfully accomplished.

2. Momentarily depress the LOCK and AM pushbuttons on the front panel. The Receiver will enter its BITE check mode as indicated by (1) the appearance of REMOTE in the LCD display; (2) the rapidly changing frequencies, modes, and LCD displays on the front panel, and (3) the presence of rapidly changing AF

tones and sounds (if AF is being monitored). BITE performs checkout procedures on the following assemblies:

A2 - First Mixer
A3 - Second Mixer
A4 - Main IF/AF
A5 (if installed) - ISB
A6A2 (memory portion) - Microcomputer
A7 - First and Third LO Synthesizers
A8 - Second LO Synthesizer
IF Bandwidth Filters

NOTE

By observing the frequency display LCD, it is possible to isolate a fault to the board level by noting BITE error code(s) which appear in that display.

3. If an error code does appear in the frequency LCD (this will consist of a two-digit number) refer to Table 5-3, BITE Error Code Identification. If more than one board is identified as a suspected fault, depress and release the LOCK and CW pushbuttons simultaneously and observe the display. A subsequent number will appear which, when considered along with the number which first appeared, should identify the faulty board.

4. Replace the faulty board and repeat steps 1 through 3 until no further faults are indicated by BITE. (This will be indicated by the exit from REMOTE and the return of the Receiver to its pre-BITE status).

Successful completion of Paragraphs 5.4.1 and 5.4.2 verify the operational readiness status of all boards except: the A1 Low Pass Filter, the A6A1 Remote Interface, and Audio portions of A4 Main IF/AF and A5 ISB (if installed).

These boards can be verified by performing the procedures in Paragraphs 5.4.3, 5.4.4, 5.4.5 and 5.4.6.

Table 5-3. BITE Error Code Identification

DISPLAYED ERROR	DESCRIPTION	PROBABLE FAULT
01	First Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.	A7
02	Second Local Oscillator (reference) synthesizer not locked.	A8
03	First Local Oscillator synthesizer does not break lock to enter fast sampling mode on 500 kHz step change.	A7
04	Third Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.	A8

Table 5-3. BITE Error Code Identification (Cont.)

DISPLAYED ERROR	DESCRIPTION	PROBABLE FAULT
05	Third Local Oscillator synthesizer not locked 100 millisecond delay from 500 kHz and 500 Hz step change, respectively. 03 and 05 indicates A7 fault; 04 & 05 by itself indicates A8 fault.	A8, A7
06	Filter slot contains a symmetrical filter, but there is/are SSB filter(s) also in the system.	Wrong or bad filter.
07	Filter slot one contains an upper sideband filter. ISB operation, if installed, will be impaired.	Wrong or bad filter.
08	No USB filter has been found in a system, and filter slot one does not contain a symmetrical filter.	Wrong or bad filter.
09	Too many symmetrical filters installed in system.	Check filters. installed.
10	Not used.	
11	No LSB filter has been found in the system and filter slot one does not contain a symmetrical filter.	Wrong or bad filter.
12	No symmetrical filters have been found in the system.	Wrong or bad filter.
13	Filter slot one does not contain a lower sideband filter, but ISB is installed. If ISB is installed and no 13 error, A5 is functional.	Wrong or bad filter.
14	Random access memory test failure: Data written to memory different from data read back.	A6A2
15	Either no filters are installed in the system, or the synthesizer signal strength is out of range prescribed for BITE. NOTE: If no 15 error, A2 A3, and A4 are fully functional.	A2
16	Filter slot one contains a filter.	Wrong or bad filter.
17	Two or more LSB filters have been found in the system.	Wrong or bad filters.

Table 5-3. BITE Error Code Identification (Cont.)

DISPLAYED ERROR	DESCRIPTION	PROBABLE FAULT
√ 18	Two or more USB filters have been found in the system.	Wrong or bad filters.
19	Although a lower sideband filter has been found in system, it is not installed in filter slot one. ISB operation, if installed will be impaired.	Wrong or bad filters.
20	Not Used.	
21	Filter in filter slot one is skewed from the IF center frequency.	*Wrong or bad filter.
22	Filter in filter slot two is skewed from the IF center frequency.	*Wrong or bad filter.
23	Filter in filter slot three is skewed from the IF center frequency.	*Wrong or bad filter.
24	Filter in filter slot four is skewed from the IF center frequency.	*Wrong or bad filter.
25	Filter in filter slot five is skewed from the IF center frequency.	*Wrong or bad filter.
26	Filter in filter slot six is skewed from the IF center frequency.	*Wrong or bad filter.
√ 27	Filter in filter slot seven is skewed from the IF center frequency.	*Wrong or bad filter.
28	Not Used.	
29	Not Used.	
30	Not Used.	
	NOTE: 31 thru 37; 80% probability of bad filter. 30% probability A4 board.	
31	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot two.	Bad filter, A4
32	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot two.	Bad filter, A4

*Synthesizer off frequency, wrong or bad filters.

Table 5-3. BITE Error Code Identification (Cont.)

DISPLAYED ERROR	DESCRIPTION	PROBABLE FAULT
33	BITE frequency sweep underflowed while attempting to measure bandwidth of filter in filter slot three.	Bad filter, A4
34	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot four.	Bad filter, A4
35	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot five.	Bad filter, A4
36	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot six.	Bad filter, A4
37	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot seven.	Bad filter, A4

* Synthesizers off frequency, or wrong or bad filters.

5.4.3 A1 Low Pass Filter Check

Connect a coaxial cable (i.e. RG 223/U) between Reference IN/OUT connector J7 and RF IN connector J1. Ensure that S2 is in the INTERNAL position. Set the receiver controls as follows:

MODE: CW
AGC: Short
BFO: +1.00 kHz
FILTER: Nearest 3.2 kHz

Using the Frequency Keypad, enter the following frequencies in order, noting that as each frequency is selected, a 1 kHz tone is present at the audio output jack: 01.000000, 05.000000, 10.000000 and 25.000000 MHz.

Should the audio tone not be heard at any of the above frequencies, the A1 Filter Assembly is possibly defective, and should be replaced.

5.4.4 A4 Main IF/AF (AF Section) Check

1. Connect J7 to J1 as described in Paragraph 5.4.3.
2. Using pushbutton frequency entry, set receiver to 01.000000 MHz.
3. Select CW, BFO +100 kHz, and 3.2 kHz (or nearest) bandpass filter.

Ensure that the AF GAIN Control has been advanced at least one third clockwise from the fully counter-clockwise position. If the A4 board audio circuitry is operative, a 1 kHz tone will be heard at the phone jack on the front panel.

4. Place the AF/RF meter in the AF mode. Using a screwdriver rotate the MAIN LINE LEVEL control, and note that the AF meter varies from -10 dBm to greater than 0 dBm. This last step will check the operation of the A4 line amplifier.

5.4.5 A5 ISB (AF Section) Check (if installed)

1. Connect J7 to J1 as described in Paragraph 5.4.3.
2. Using pushbutton frequency entry, set receiver to 01.001000 MHz.
3. Select ISB/L from the Mode panel. Ensure that the AF GAIN control has been advanced at least one-third clockwise rotation from the fully off position. If the A5 board is operative, a 1 kHz tone will be heard at the phone jack on the front panel.
4. Place the RF/AF meter in the AF mode. Using a screwdriver rotate the I-LSB LINE LEVEL control and note that the AF meter varies -10 dBm to greater than 0 dBm. This last step will check the operation of the ISB line amplifier.

5.4.6 A6A1 Remote Serial Asynchronous Interface Check (if installed)

1. Ensure that all previous paragraphs have been successfully accomplished.
2. Connect a suitably wired remote terminal to the Receiver via connector A6A1W1J1 on the rear panel.
3. Enter $99GCR on the terminal keyboard and observe the results on the remote display. If data is displayed, A6A1 is functional. If data is not displayed, A6A1 is faulty and must be replaced.

NOTE

99 represents the receiver number. If the receiver number is different, enter the desired number instead of 99.

This completes the Operational Checkout and Fault Isolation Procedures for the RA6793A Receiver.

5.5 RA6793A PERFORMANCE TESTS

RA6793A performance tests can be most effectively carried out if the technician gains some degree of familiarization with the operating instructions and circuit descriptions provided in Sections III and IV, respectively. Parts lists and component location diagrams are located in Section VI.

These performance test procedures may be used for initial inspection, periodic checks and to confirm performance specifications after repairs have been made. These tests determine Synthesizer performance, Audio Power and Distortion, Gain Modes, and Final IF Frequency. The tests should be conducted only by skilled technicians using the equipment listed in Table 5-2.

All tests should be conducted using Figure 5-1 as a standard test set-up. Equipment should be allowed a warm-up period of at least 30 minutes prior to conducting the test. If the Receiver does not satisfactorily pass a test, refer to Paragraph 5.6, Board Level Fault Isolation.

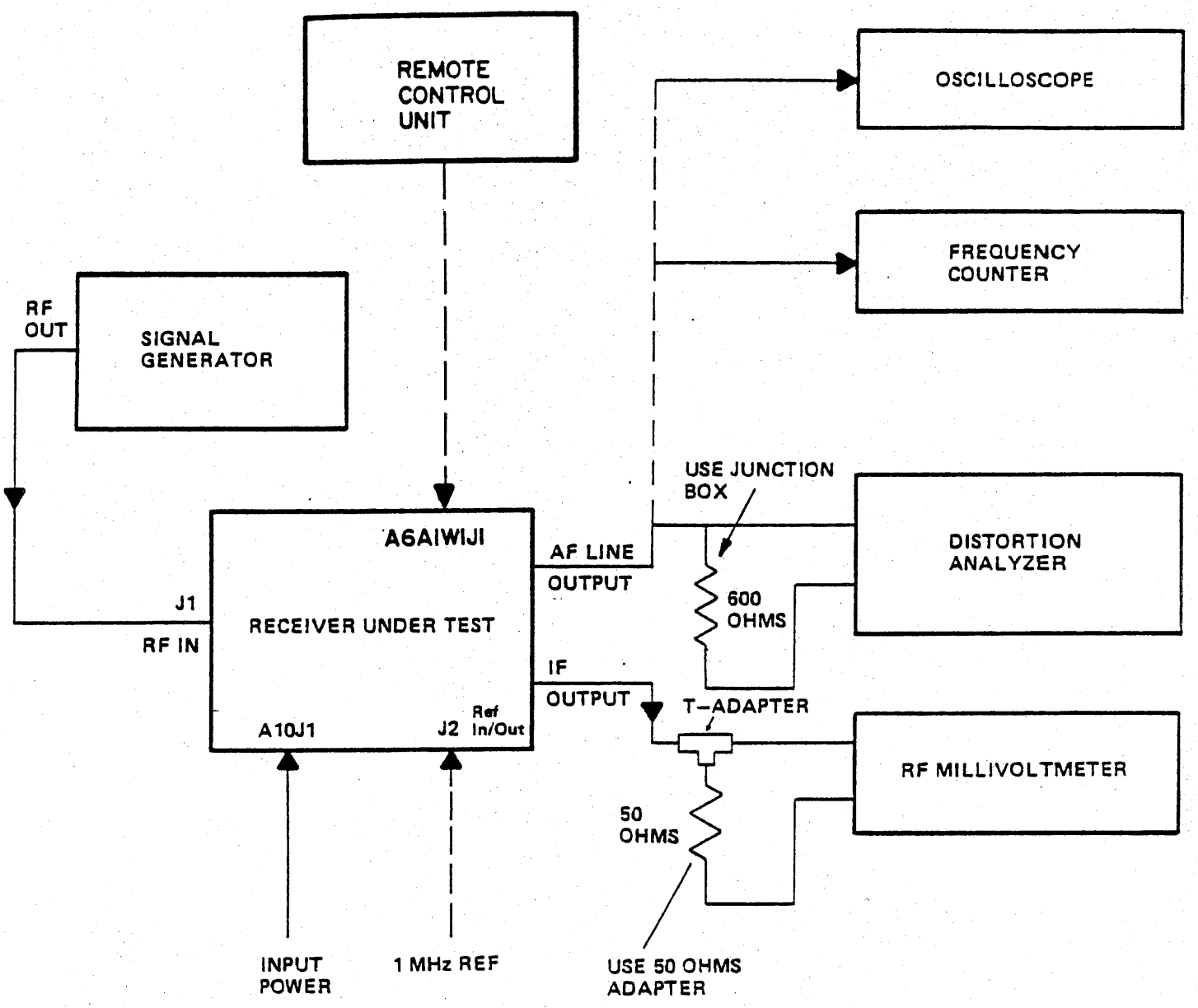


Figure 5-1. Standard Test Equipment Configuration

5.5.1 Frequency Tuning

1. Connect the receiver and test equipment as shown in Figure 5-1.
2. Set the receiver as follows:
   a. Frequency: As required in Table 5-4
   b. Mode: CW
   c. BFO: 1000 Hz
   d. AGC: Short
   e. Bandwidth: 5 kHz (or closest Bandwidth available)
3. Set the signal generator as follows:
   a. Frequency: As required in Table 5-4
   b. Level: -60 dBm, unmodulated
4. Set the Receiver and generator to the frequencies listed in Table 5-4. Ensure that the output frequency indicated by the counter remains within the limits 1 kHz ±10 Hz at each setting.

Table 5-4. Tuned Frequencies

RECEIVER/GENERATOR TUNED FREQUENCY	AF OUTPUT
00.500000 MHz	1000 ±10 Hz
01.000000	1000 ±10 Hz
11.111111	1000 ±10 Hz
22.222222	1000 ±10 Hz
23.333333	1000 ±10 Hz
24.444444	1000 ±10 Hz
25.555555	1000 ±10 Hz
26.666666	1000 ±10 Hz
27.777777	1000 ±10 Hz
28.888888	1000 ±10 Hz
29.999999	1000 ±10 Hz

5.5.2 Frequency Display

1. Set up the equipment as in Figure 5-1.
2. Set the signal generator as follows:
   a. Frequency: 1.5 MHz
   b. Mode: CW
   c. Level: -100 dBm
3. Tune the Receiver to 1.5 MHz using manual gain mode, 3.24 kHz BW; CW; at -1.8 kHz BFO offset.
4. Ensure that frequency readout display is clearly visible from a distance of 3 feet.
5. Ensure that it is possible to tune to another frequency in the same frequency band.
6. Select tuning LOCK and ensure that frequency is not changed by further rotation of tuning knob.

5.5.3 Frequency Stability

1. Connect the frequency counter to the output of REF IN/OUT J2.
2. Ensure the output frequency is 1 MHz ±1 Hz.

5.5.4 Frequency Calibration Resolution

1. Connect the frequency counter to internal standard (A8TP10).
2. Ensure that the internal standard is 5 MHz ±1 Hz.

5.5.5 RF Gain Control

1. Set up the equipment as in Figure 5-1.
2. Set the Receiver controls as follows:
   a. Power: ON
   b. Gain Mode: Manual
   c. Detection Mode: CW
   d. BW: 3.24 kHz
3. Set the signal generator for an output of 1.5 MHz at -100 dBm, CW. Connect signal generator to RF IN connector J1 on rear panel.
4. Using the remote controller, adjust the manual gain control on the receiver fully clockwise and adjust the line level control for 1 mW output on distortion analyzer.
5. Adjust the manual gain control on the remote control device one step down and check whether or not the AF output falls by 3 ± 1.5 dB.
6. Increase signal generator level to 1 mW and repeat step 5 until manual gain is at minimum.
7. Restore the 1 mW reference at the minimum manual gain and note the signal generator level. This should be greater than -10 dBm.

5.5.6 Final IF Frequency

1. Set up the equipment as shown in Figure 5-1.
2. Set the Receiver controls as follows:
   a. Power: ON
   b. Gain Mode: AGC-SHORT
   c. BW: 3.2 kHz
   d. Receiver Tuned Frequency: 1.5 MHz
   e. Detection Mode: CW
3. Set the signal generator for an output of 1.5 MHz, CW at a level of -100 dBm.
4. Note the IF output level indicated on the RF voltmeter.
5. Remove the 50 ohm load from the IF output and observe that the indicated output voltage increases by 6 dB ±1 dB.
6. Connect the frequency counter to IF output jack J2 and measure the IF frequency. This should be 455.000 kHz.

5.5.7 Fixed and Variable BFO Operation

1. Set the Receiver controls as follows:
   a. Power: ON
   b. Gain Mode: N/A
   c. Detection Mode: CW
   d. BW: N/A
   e. BFO: ON (word BFO displayed in Mode LCD)
2. Disconnect the A4 module by removing W10P1.
3. Connect the frequency counter to A4J6 to monitor the BFO frequency.
4. Using the Receiver front panel controls, select each BFO indication listed in BFO Indicator column of Table 5-5 and verify the frequencies listed in BFO Frequency Column are obtained.

5. Select USB and LSB modes and observe the BFO frequency is 455.000 kHz. (SSB/ISB receivers fitted with 08409 and 08410 option filters only).
6. Disconnect frequency counter and reconnect W10P1 to A4 module.

Table 5-5. BFO Test Values

BFO INDICATOR	BFO FREQUENCY
0.00 kHz	455.00 kHz
+1.11	453.890
2.22	452.780
3.33	451.670
4.44	450.560
5.55	449.450
6.66	448.340
7.88	447.120
7.99	447.010
-1.11	456.110
-2.22	457.220
-3.33	458.330
-4.44	459.440
-5.55	460.550
-6.66	461.660
-7.77	462.770
-7.88	462.880
-7.99	462.990

5.5.8 Audio Output Power

1. Set up test equipment as shown in Figure 5-1.
2. Set Receiver controls as follows:
   a. Power: ON
   b. Gain Mode: AGC-SHORT
   c. BW: 3.24 kHz
   d. Detection Mode: CW
   e. Receiver Tuned Frequency: 1.5 MHz
3. Set the signal generator for an output of 1.5 MHz at -97 dBm, CW.
4. Tune the signal generator (or receiver) to produce an AF output of 1.8 kHz ± 50 Hz as indicated on the Frequency Counter.
5. Set the AF output level to 1 milliwatt using the LINE LEVEL control on the Receiver front panel and phone output.
6. Select Receiver bandwidth of 6.8 kHz and AM detector mode. Amplitude modulate the input signal 30% at 1 kHz.
7. Observe that the AF output level is within 5 dB of the reference set in step 5 for both line output and phone output.
8. Slowly rotate the AF gain control through the control range. Observe that the phone output level varies smoothly over the full control range.

5.5.9 Audio Distortion

1. Set up the equipment as shown in Figure 5-1.

2. Set Receiver controls as follows:
   a. Power: ON
   b. Gain Mode: Manual Gain
   c. Detection Mode: CW
   d. BW: 3.24 kHz
   e. BFO: -1.00 kHz
   f. Receiver Tuned Frequency: 1.5 MHz
3. Set the signal generator for an output of 1.5 MHz at -47 dBm, CW.
4. Adjust manual gain control for 1 mW output. Measure distortion. Distortion should be less than 2%.
5. Connect phone output from Receiver front panel to distortion analyzer and adjust phone output for 10 mW. Measure distortion. Distortion should be less than 3%.

5.5.10 Operation After Restoration of Power.

1. Carefully note the Receiver tuned frequency, BW and other displayed functions on Receiver front panel and de-energize the Receiver.
2. After 1/2 hour, energize the Receiver and ensure that the Receiver returns to the display noted in step 1.

5.6 BOARD LEVEL FAULT ISOLATION

Figure 5-2 along with Table 5-6 shows signal flow between individual circuit cards, and the jacks and/or test points for measuring signal values. Table 5-7 presents some typical front panel fault symptom data. This information, along with the BITE check detailed in Paragraph 5.4.2 and the Performance Tests detailed in Paragraph 5.5 should be used in isolating malfunctions to the board level. Receiver settings, signal generator settings, and connector pin location diagrams are shown as part of Figure 5-2. The following procedures should be used to perform signal level tests:

1. Set signal generator outputs as specified in Figure 5-2.
2. Set receiver front panel controls as specified in Figure 5-2.
3. Measure values indicated at each jack or test point using appropriate test equipment.
4. Tolerances are: $\pm$ 3 dBm; $\pm$ 0.5 volts.

Once a fault has been isolated, the faulty circuit card should be replaced in accordance with the Receiver Assembly and Disassembly procedures detailed in Paragraph 5.7; and Receiver proper operation verified. Verification is accomplished by performing BITE check (Paragraph 5.4.2) and Performance Tests (Paragraph 5.5).

5.6.1 Fault Isolation Test Table

Table 5-6 lists the signal values present at the test points and significant points of measurement in the Receiver. Unless otherwise stated, the measurements were made with the Receiver set as described in subparagraphs a and b. For convenience the circuit cards are grouped in the Table as they are in the Receiver.

a. Maximum Gain Test Set-Up. The Receiver to be tested should be placed on a convenient work bench. The top and bottom covers of the Receiver and the individual module covers should be removed to gain access to the test points. Set the signal generator to produce a 5.5 MHz signal at an output level of -50 dBm. Connect the signal generator output to the RF INPUT on the Receiver (rear panel connector J1). Tune the Receiver

TABLE 5-6. FAULT ISOLATION TEST TABLE

Step	Connection of Test Equipment		Point of Test	Control Settings	Performance Standards
		FIRST MIXER, CIRCUIT CARD ASSEMBLY A2			
1	Spectrum Analyzer		A2TP1		+6 dBm, ±3dB 45.955 MHz
2	with High Z Probe		A2TP2		+5 dBm, ±3 dB 45.955 MHz
3	Center Frequency:	45.955 MHz	A2TP3		+8 dBm, 45.955 MHz
4	Output level:	+10 dBm	A2E1		-51 dBm, ±3 dB 5.5 MHz
5	Input Attenuator:	20 dB	A2E3		-51 dBm, ±3 dB 5.5 MHz
6	Log Reference Level:	10 dBm, 10 dB/Log	A2E8		-51 dBm, ±3 dB 40.455 MHz
	Bandwidth:	300 kHz			
	Scanwidth:	1 MHz/Div			
7	Digital Multimeter:		A2TP4		0.57 ±0.05 Volts dc
8			A2TP4		+11.6 ±0.15 Volts dc
		SECOND MIXER, CIRCUIT CARD ASSEMBLY A3			
9	Spectrum Analyzer		A3E1		-55 dBm, ±3 dB 40.455 MHz
10	with High Z Probe		A3E3		-50 dBm, ±3 dB 40.455 MHz
11	Center Frequency:	40.455 MHz	A3TP1		-34 dBm, ±3 dB 40.455 MHz
12	Output Level:	-50 dBm	A3TP2		-25 dBm, ±3 dB 455 kHz
14	Input Attenuator:	10 dB	A3TP3		-18 dBm, ±3 dB 455 kHz
15	Log Reference Level:	0 dB, 10 dB/Log			0 dBm, ±3 dB 455 kHz
	Bandwidth:	300 kHz			
	Scanwidth:	1 MHz/Div			
	Scan Time:	20 Msec/Div			
	Video Filter:	10 kHz			
		FIRST LO SYNTHESIZER, CIRCUIT CARD ASSEMBLY A7			
16	Digital Multimeter		A7TP1	Reset Receiver	+5 ±0.2 Volts, dc
17			A7TP5	to CW mode	+5.2 ±0.05 Volts, dc
18			A7TP2	(if necessary)	Ground
19	Oscilloscope		A7TP3		4 V p-p random digital sig.
20	with X10 Probe		A7TP3		4 V p-p random digital sig.
21			A7TP4		4 V p-p random digital sig.
22			A7TP6		5 V negative going pulses, kHz
23			A7TP7		1 V negative going pulse
24	Digital Multimeter		A7TP8		1 V narrow pulse, negative going
25			A7TP9		+8.1 ±0.5 Volts, dc
26			A7TP10		+5.2 ±0.5 Volts, dc
27			A7TP11		+5.2 ±0.5 Volts, dc
28			A7TP12		+5.2 ±0.5 Volts, dc
29			A7TP13		+0.2 ±0.1 volts, dc

TABLE 5-6. FAULT ISOLATION TEST TABLE

Step	Connection of Test Equipment		Point of Test	Control Settings	Performance Standards
	SECOND LO/BFO SYNTHESIZER, CIRCUIT CARD ASSEMBLY A8				
30	Oscilloscope with		A8TP10		4 Volts p-p, 5 MHz
31	X10 Probe		A8TP1		5 Volts p-p, 5 MHz
32			A8TP2		4 Volts p-p, 5 MHz
33			A8TP3		4 Volt Negative going pulse, 5 MHz
34			A8TP4		4 Volt Negative going pulse, 5 MHz
35	Digital Multimeter		A8TP5		3.2 to 7.5 Volts dc
36			A8TP11		0.4 Volts dc maximum
37			A8TP12		0.4 Volts dc maximum
38	Oscilloscope with		A8TP6		5 Volt Negative going pulse, 500 Hz
39	X10 Probe		A8TP7		5 Volt negative going pulse, 500 Hz
40	Digital Multimeter		A8TP8		3.2 to 7.5 Volts dc
41	X10 Probe		A8TP9		0.25 Volts p-p mimimum, 22.70 MHz
	MAIN IF/AF, CIRCUIT CARD ASSEMBLY A4				
	Spectrum Analyzer		A4TP1		-38 dBm, ±3 dB, 455 kHz
42	with High Z Probe		A4TP2		-38 dBm, ±3 dB, 455 kHz
43	Center Frequency:	455 kHz	A4TP6		0 dBm, ±3 dB, 455 kHz
44	Output Level:	-50 dBm	A4TP7		0 dBm, ±3 dB, 455 kHz
45	Input Attenuator:	10 dB			
	Log Reference Level:	0 dB, 10 dB/Log			
	Bandwidth:	1200 Hz			
	Scanwidth:	0.5 kHz/div			
	Scan Time:	.5 Seconds			
	Video Filter:	100 Hz			
46	Digital Multimeter		A4TP3		+0.9 ±0.05 Volts dc
47			A4TP4		+12.7 ±0.3 Volts dc
48			A4TP5		+0.9 ±0.05 Volts dc
49			A4TP8		+6.8 ±0.3 Volts dc
50			A4TP9		+6.8 ±0.3 Volts dc
51			A4TP10		+0.6 ±0.04 Volts dc
52			A4TP11		+5.7 ±0.8 Volts dc
53			A4TP14		+6.5 ±0.8 Volts dc
54			A4TP13		1.5 Volts p-p, 454 kHz
55			A4TP15		1.4 V p-p,1 kHz (with high
56			A4TP16	LINE and AF	1.4 V p-p,1 kHz freq.comp.
57			A4TP17	GAIN controls max clockwise	1.2 V p-p,1 kHz sinewave

TABLE 5-6. FAULT ISOLATION TEST TABLE

Step	Connection of Test Equipment		Point of Test	Control Settings	Performance Standards
	ISB IF/AF, CIRCUIT CARD ASSEMBLY A5 (If Installed - Optional)				
58	Spectrum Analyzer		A5TP1	Receiver must	-38 dBm, 456.8 kHz
59	with High Z Probe		A5TP2	be set to the	-38 dBm, 455 kHz
60	Center Frequency:	455 kHz	A5TP6	ISB mode and	0 dBm, 455 kHz
61	Output Level:	-54 dBm	A5TP7	generator set	0 dBm, 455 kHz
	Input Attenuator:	10 dB		to 5.4982 MHz	
	Log Reference Level:	0 dB, 10 dB/Log			
	Bandwidth:	3 kHz/Div			
	Scandwidth:	20 kHz/Div			
	Scan Time:	.5 Seconds			
	Video Filter:	100 Hz			
62	Digital Multimeter		A5TP4		+0.9 Volts dc ±0.05
63			A5TP5		+12.7 Volts dc ±0.3
64			A5TP8		+6.8 Volts dc ±0.3
65			A5TP9		+6.8 Volts dc ±0.3
66			A5TP10		1.5 Volts p-p, 454 kHz
67			A5TP13		1.4 Volts p-p, 1 kHz
68			A5TP11		No level present
69			A5TP12	I-LSB LINE control max. clockwise	1.4 Volts p-p, 1 kHz

Table 5-7. Operationally Based Fault Symptom Chart

FAULT SYMPTOMS	BOARD/MODULE PROBABLY FAULT A1 A2 A3 A4 A5 A6 A6A1 A7 A8 A9 A10 Check Module Board According to Number Order											COMMENTS & NOTES
Unable to energize Receiver											1	Check Power Supply
MODE LCDs blank mostly zeros in Frequency LCD						2						PC wafer in wrong position, A6A2
Unable to establish LOCAL operating condition						1				2		A6A2, A9
FAULT LED illuminated								1	2			Synthesizer failure, A7, A8, S2 switch in wrong position.
BITE error code display												See BITE error code chart
Unable to exit LOCK Mode						2				1		A9, A6A2
No manual tuning										1		A9
No meter level indication in AF or RF	2			1								A4, A1
No audio output				1								A4
No audio output ISB only					1							A5
Unable to adjust Line Level Out				1								A4
No Remote Data entry/return							1					A6A1
No tone from BFO in CW mode									1			A8 - Confirm CW signal present and not in BFO CENTER

Table 5-7. Operationally Based Fault Symptom Chart (Cont.)

FAULT SYMPTOMS	BOARD/MODULE PROBABLY FAULT A1 A2 A3 A4 A5 A6 A6A1 A7 A8 A9 A10 Check Module Board According to Number Order											COMMENTS & NOTES
Displayed IF bandwidth does not match any installed filter				2								Check filters, A4
Unable to enter frequency from receiver front panel						3				2		Confirm Receiver not in Remote
IF output at J2 not at 455 kHz						3		2	1			A8, A7, A4
Unable to initialize BITE routine						2				1		Confirm Receiver not in Remote
Receiver does not retain frequency data after Power Interrupt						1						Check Battery

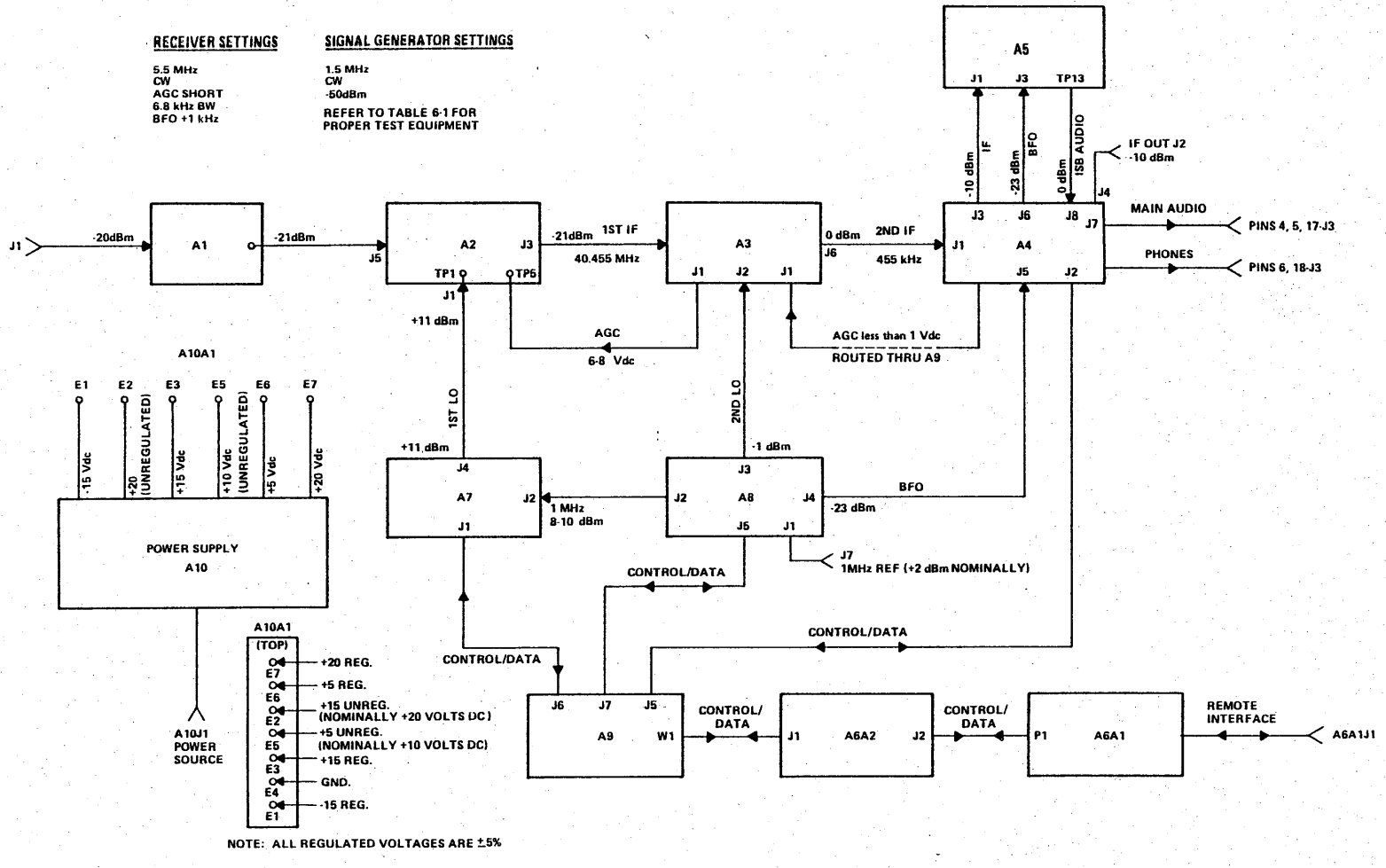


Figure 5-2. Typical Signal Levels RA6793A HF Receiver

frequency to 5.5 MHz. Select the CW operating mode and adjust the BFO to provide a +1.00 kHz offset. Select an IF filter as close as possible to 3.2 kHz bandwidth. Set the AGC to the MAN operating mode and IF GAIN control to maximum clockwise position. Ensure Receiver is operating from own internal reference. Set switch S2, on rear panel to INT position.

b. AGC Test Set-Up. All procedures for AGC test set-up are the same as Paragraph a, except set AGC to SHORT operating mode.

5.6.2 Operational Fault Symptom Chart

Table 5-7 contains typical operational fault symptoms and their most probable causes. The Table should be used as a guideline only, and should be supplemented with the BITE check detailed in Paragraph 5.4.2 and the Performance Tests detailed in Paragraph 5.5.

5.7 RECEIVER ASSEMBLY AND DISASSEMBLY PROCEDURES

The followng paragraphs outline the procedures for removal and installation of the individual circuit card assemblies used in the RA6793A HF Receiver. A complete list of these assemblies is contained in SECTION VI, Replacement Parts List, of this instruction manual.

5.7.1 Preliminary Procedure

Prior to removing or installing any assembly it is necessary to disconnect the receiver from its power source. It is also necessary to remove the Receiver from the system (except to replace the fuse).

NOTE

Ensure that all system cables are disconnected from the Receiver prior to removing the Receiver from its mounts. Place the Receiver on a suitable work space large enough to allow for positioning the Receiver either horizontally or vertically as required for removal of the desired board. The only tools required for LRU removal or installation are a flat-blade screwdriver and a screw starter. Adequate light should be available for ease in reading internal cable, jack, and connector numbers, and for aligning LRU mounting holes with corresponding mounting fixtures on the Receiver chassis.

CAUTION

Do not expose the Receiver to direct ultraviolet light while performing the following steps. Such exposure may cause erasure of data stored in the EPROMS.

5.7.2 Top and Bottom Covers

If boards A2, A3, A7, or A8 are to be removed or installed, only the Receiver's bottom cover must be removed for access. If boards A4, A5, A6A1, A6A2 or A10 are to be removed or installed, only the receiver's top cover must be removed for access. If boards A1 or A9 are to be removed or installed, both the Receiver's bottom and top covers must be removed for access. The procedure for removing either cover is as follows:

1. Position the Receiver horizontally so that the cover to be removed is up.
2. Loosen (counterclockwise) the six (6) 1/4 turn fasteners located on the cover.
3. Carefully lift the cover by its edges and remove it from the Receiver.

Installation of either cover is as follows:

1. Position the cover on the Receiver so that the six (6) 1/4 turn fasteners on the cover align with their mounting holes on the Receiver, and so that the front edge of the cover is inserted into the slot on the rear of the front panel.
2. Apply a small amount of hand pressure to the cover to engage the fastener with its mount.
3. Tighten (clockwise) the six (6) fasteners 1/4 turn.

5.7.3 A1 Module Removal

CAUTION

Do not allow the A1 module to drop when the screws are removed. Failure to do so may cause damage to the A1 module or to the Receiver.

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1
2. Remove both the Receiver top and bottom covers as directed in Paragraph 5.7.2.
3. Disconnect SMB connector A1W2P1 from J5 on the receiver frame.
4. Disconnect BNC connector A1W1J1 from J1 (the RF IN jack) on the rear panel.
5. Stand the Receiver on its side.
6. Working from the bottom of the Receiver, loosen and remove the two screws and hardware from the ends of the A1 module.

5.7.4 A1 Module Installation

Installation is the reverse of removal with the following notes:

1. The end of the A1 module marked "IN", when positioned correctly, is mounted on the mount nearest S2 (EXT-INT REF switch).
2. When installing the mounting screw at the "IN" end, ensure that the ground lug on the A1W1J1 cable is placed inside the A1 module between the A1 cover and the threaded mount, and that the mounting screw goes through the lug.

5.7.5 A2 Module Removal

CAUTION

Bumping J5 or the capacitors may cause damage to the A2 module printed circuit track or components.

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver bottom cover as directed in Paragraph 5.7.2.
3. Remove the six (6) screws and hardware which hold down the A2 module cover.
4. Remove the A2 module cover.
5. Disconnect eight-pin connector W21P1 from A2J2.
6. Disconnect SMB connector W2P1 from A2J1.
7. Disconnect SMB connector W1P1 from J5 on the receiver frame.
8. Disconnect SMB connector A3W1P1 from A2J3.
9. Loosen and remove the six (6) screws and hardware which hold down the A2 module.
10. Lift out the A2 module tipping it slightly to avoid bumping the module against J5 and the four (4) feed-through capacitors located on the side of the Receiver frame.

5.7.6 A2 Module Installation

Installation of the A2 module is the reverse of removal with the following notes:

1. Ensure cable W2P1 is located near the notch in the receiver frame when installing the module.
2. Ensure that the cable connected to W2P1 (coming from the A7 module area) is routed through the notch on the edge of the receiver frame. Failure to do so may result in damage to the cable.

5.7.7 A3 Module Removal

CAUTION

Bumping J6 or the capacitors may cause damage to the A3 module printed circuit track or components.

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver bottom cover as directed in Paragraph 5.7.2.
3. Using the pull-tab on the A3 module cover, carefully remove the A3 cover.
4. Disconnect eight-pin connector W22P1 from A3J1.
5. Disconnect SMB connector A3W2P1 from J6 on the receiver frame.
6. Disconnect SMB connector W4P1 from A3J2.
7. Loosen and remove the six (6) screws and hardware which hold down the A2 module cover.
8. Remove the A2 module cover.
9. Disconnect SMB connector A2W1P1 from A2J3 on the A2 module.
10. Loosen and remove the six (6) screws and hardware which hold down the A3 module.
11. Lift out the A3 module tipping it slightly to avoid bumping the module against J2 and the five (5) feed-through capacitors located on the side of the receiver frame.

5.7.8 A3 Module Installation

CAUTION

Ensure cable A3W1P1 is routed through the notch in the frame prior to installation of both the A2 and A3 module covers. Failure to do so may result in damage to the cable.

Installation of A3 module is the reverse of removal with the following note:

NOTE

Ensure cable A3W1P1 is located near the notch in the Receiver frame when installing the module.

5.7.9 A4 Module Removal

NOTE

The two (2) screws which hold down transformer T1 to the A4 module do not need to be removed to remove the module nor does the screw through U27. Eight (8) hold down screws are located around the A4 module edges, and the two (2) additional screws are located in the middle area of the module.

1. Perform the Preliminary Procedures as directed in Paragraph 5.7.1.
2. Remove the Receiver top cover as directed in Paragraph 5.7.2.
3. Remove the Bandwidth Filter cover and optional crystal Bandwidth Filters (if installed) as directed in Paragraph 5.7.22.1.
4. Disconnect SMB connector W1P2 from A4J1.
5. Disconnect SMB connector W11P1 from A4J3.
6. Disconnect SMB connector W12P1 from A4J4.
7. Disconnect SMB connector W6P2 from A4J5.
8. Disconnect SMB connector W10P1 from A4J6.
9. Disconnect ribbon connector A5W1P1 from A4J8.
10. Disconnect ribbon connector W16P1 from A4J7.
11. Disconnect ribbon connector W15P1 from A4J2.
12. Loosen and remove the twelve (12) screws and hardware which hold down the A4 module.
13. Lift out the A4 module.

5.7.10 A4 Module Installation

CAUTION

Ensure that all cables and connectors are clear of the A4 module during installation. Failure to do so may result in having to remove the module again to properly position the cables.

Installation of the A4 module is the reverse of removal with the following note:

NOTE

When positioning the A4 module for installation, the Bandwidth Filter slots (labeled FL1-FL7 on the A4 module) are located toward the side of the Receiver nearest the A10 (Power Supply) module.

5.7.11 A5 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver top cover as directed in Paragraph 5.7.2.
3. Disconnect ribbon connector A5W1P1 from A4J8.

NOTE

The connector disconnects from the A4 module, not the A5 module, and the ribbon cable is part of the A5 module.

4. Disconnect SMB connector W10P2 from A5J3.
5. Disconnect SMB connector W11P2 from A5J1.
6. Loosen and remove the four (4) mounting screws and hardware from the four corners of the A5 module.
7. Lift out the A5 module.

5.7.12 A5 Module Installation

Installation of the A5 module is the reverse of removal.

5.7.13 A6 Module Removal

1. Perform the Preliminary Procedures as directed in Paragraph 5.7.1.
2. Remove the Receiver top cover as directed in Paragraph 5.7.2.
3. Disconnect ribbon connector A9W1P2 from A6J1.
4. From outside the rear panel, loosen and remove the two (2) screws and hardware that hold A6A1W1J1 to the rear panel.
5. Loosen and remove the six (6) screws and hardware that hold the upper edge of the A6 module to the side of the Receiver.

NOTE

The A6 module is composed of two separate (when the optional A6A1 is installed) printed circuit boards, A6A1 and A6A2, joined in the middle by A6P1 which is a fifty (50) pin connector. If it is desired to separate the two boards, grasp one board in each hand and carefully pull them straight apart.

CAUTION

Failure to exercise care may result in damage to the connector

CAUTION

After removing the A6A2 module, do not place it on a conductive surface as this may cause damage to the battery on the A6A2 module.

6. Carefully lift out the A6 module.

5.7.14 A6 Module Installation

CAUTION

When joining the optional A6A1 and A6A2 together, ensure that the P1 connector holes and pins are correctly aligned with each other prior to applying pressure. Failure to do so may result in damage to the connector.

Installation of the A6 module is the reverse of removal with the following notes:

1. When installing the A6 module into the Receiver, ensure that A6A1W1J1 is located in the cutout on the rear panel, and the bottom edge of the module is in the nylon track on the Receiver frame.
2. For ease of installation, install the second screw from the rear panel with its nylon washer if installed (between the A6A1 module and the mounting post) first.

5.7.15 A7 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver bottom cover as directed in Paragraph 5.7.2.
3. Loosen and remove the single screw and hardware that holds down the A7 module cover.
4. Using the pull-tab on the A7 module cover, remove the A7 module cover.
5. Disconnect ribbon connector W13P1 from A7J1.
6. Disconnect SMB connector W3P1 from A7J2.
7. Disconnect SMB connector W2P2 from A7J4.
8. Loosen and remove the eleven (11) screws and hardware, and the nylon mounting post (from which the A7 module cover screw was removed in Step 3 above) which holds down the A7 module.

NOTE

The screw through A7U39 is <u>not</u> a module holddown screw. The screw through the heatsink bracket on regulator A7Q4 <u>is</u> a module holdown screw. When removing the screw through A7Q4 take care not to bend or damage the regulator.

9. Lift out the A7 module.

5.7.16 A7 Module Installation

Installation of the A7 module is the reverse of removal with the following notes:

1. When positioning the A7 module for installation, ensure that ribbon connector A751 is located next to the cutout in the Receiver frame.
2. When installing the screw through A7Q4, heatsink bracket. Take care that it is centered on the mounting hole.

5.7.17 A8 Module Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver bottom cover as directed in Paragraph 5.7.2.
3. Using the pull-tab on the A8 module cover, remove the A8 module cover.
4. Disconnect ribbon connector W14P1 from A8J5.
5. Disconnect SMB connector W7P1 from A8J1.
6. Disconnect SMB connector W6P1 from A8J4.
7. Disconnect SMB connector W3P2 from A8J2.
8. Disconnect SMB connector W4P2 from A8J3.
9. Remove the eight (8) screws and hardware which hold down the A8 module.
10. Lift out the A8 module.

5.7.18 A8 Module Installation

CAUTION

Before installing the A8 module cover, ensure that all cables entering the A8 area are routed through their cutouts in the receiver frame. Failure to do so may result in damage to the cables.

Installation of the A8 module is the reverse of removal with the following note:

NOTE

When positioning the A8 module for installation, ensure that ribbon connector jack J5 is located next to the cutout in the receiver frame.

5.7.19 A9 Module Removal, Inspection and Installation

The three circuit cards A9A1, A9A2 and A9A3 making up the A9 assembly are installed on the front panel assembly which includes the front panel, encoder assembly, keypads, edgelighting, LCD's and other controls and switches. The disassembly, inspection and reassembly of the front panel assembly must be accomplished in order to remove the two circuit cards, requiring intricate procedures. These procedures are included in Paragraph 5.8 of this section under Special Maintenance.

5.7.20 A10 Module Removal

NOTE

Take care not to crush the A10J2 or A10J3 connectors, the cooling fins on A10U1 or A10U2, or to snag the W12 wire which connects to A4J1.

WARNING

The filter capacitors used in the power supply will retain an electrical charge after power is removed. The capacitors should be discharged slowly by shorting the terminals through a protected resistive device.

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver top cover as directed in Paragraph 5.7.2.
3. Loosen (counterclockwise) the four (4) 1/4 turn fasteners on the A10 module cover.
4. Lift out the A10 module cover.
5. Remove the Bandwidth Filter cover as directed in Paragraph 5.7.22.1.
6. Disengage the locking clips (2 each) on connectors A10J2 and A10J3 located on the outside of the A10 module.
7. Carefully unplug the connectors from A10J2 and A10J3.
8. Loosen and remove the five (5) screws and hardware (located on the outside of the rear panel) which hold the back panel of the A10 module to the rear panel of the receiver. Loosen the four captive screws at the base of the A10 module.
9. Grasping the sides of the A10 module, slide the module away from the rear panel while lifting the end of the A10 module nearest the Bandwidth Filters and lift out the A10 module.

5.7.21 A10 Module Installation

Installation of the A10 module is the reverse of removal with the following cautions:

CAUTION

Move ribbon connectors W19P3 and W20P1 out of the way when installing the A10 module. Failure to do so may result in damage to the A4 module or the cooling fins on the rear of the A10 module.

CAUTION

When installing the A10 module cover, ensure that the lower edge of the cover clears the nylon cable clamp on the small ribbon cable joining W19P3. Failure to do so may cause damage to the cable, cable clamp, or A10 module cover.

5.7.22 IF Bandwidth Filter Removal and Installation (For Optional Crystal Filters)

5.7.22.1 Bandwidth Filter Removal

1. Perform the Preliminary Procedure as directed in Paragraph 5.7.1.
2. Remove the Receiver top cover as directed in Paragraph 5.7.2.
3. Loosen the two (2) captive screws in the Bandwidth Filter Cover (nearest the Receiver frame) which hold the cover to the A4 module.
4. Loosen and remove the one (1) non-captive screw in the Bandwidth Filter Cover (on the side opposite the two captive screws). Be careful not to lose the lockwasher and flatwasher which fit between the Bandwidth Filter cover and the A4 module.
5. Lift off the Bandwidth Filter cover.

6. Grasp the filter to be removed between thumb and forefinger. With a gentle side-to-side rocking motion, carefully work the filter out of its slot in the A4 module.
7. Repeat step 6 for each filter to be removed making note of which filter is installed in each slot.

5.7.22.2 Bandwidth Filter Installation

Installation of the optional crystal Bandwidth Filters is the reverse of removal with the following note:

NOTE

If the Receiver is to be operated with the ISB option, both upper and lower sideband filters must be installed in the Receiver. Additionally, the lower sideband filter must be installed in the FL1 position. If the Receiver is not to be operated with the ISB option, either a lower sideband filter or symmetrical sideband filter may be installed in the FL1 position. If a lower sideband filter is installed, the companion upper sideband filter must also be installed in one of the remaining filter positions. If a symmetrical sideband filter is used, the Receiver will use the filter installed in the FL1 position for both sidebands by making the appropriate frequency offsets to the first and second local oscillators.

The remaining filters may be installed in any sequence in filter positions FL2 through FL7. However, in order to simplify system operation and troubleshooting, it is recommended that a format be established and used for all Receivers at a particular site. A typical format would be to insert the USB filter (if used) in position FL2 and insert filters with increasing bandwidths in filter positions 3 through 7.

Once the filter complement and arrangement has been determined, the following procedure should be used to insert the filters into the Receiver:

1. Working from the front of the receiver, position the filter to be used for LSB operation over filter position FL1 (the filter position closest to the rear of the receiver). Make certain that the large pins are aligned with the large sockets and the smaller pins are aligned with the smaller sockets.
2. Carefully push down on the filter to insert the pins into the sockets. Relatively light pressure is required to insert the pins into the sockets. If the filter does not easily slide into place, recheck the pin/socket alignments.
3. Insert the appropriate filters into filter positions FL2 through FL7 (as required), using the procedures described in steps 1 and 2.
4. After all filters have been inserted, visually inspect the filters to insure that they are properly seated. The bottom of the filters should be flat against the surface of the A4 board.
5. Replace the RF shield over the filters and secure the shield in place by tightening the three screws.

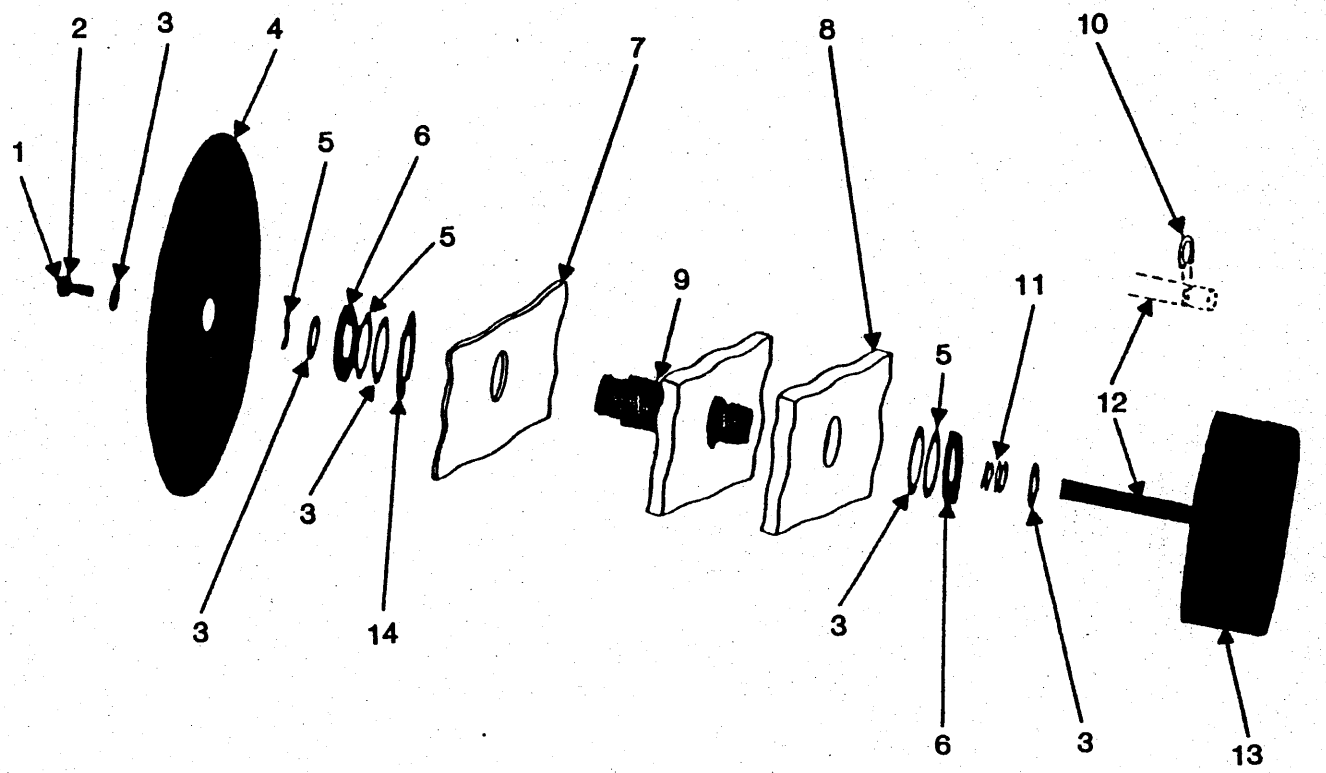
5.8 SPECIAL MAINTENANCE

5.8.1 Front Panel Assembly

The front panel assembly contains the A9A1, A9A2 and A9A3 circuit cards, encoder assembly, and other mechanically operated controls that can deteriorate during normal use. Refer to Figures 5-3 and 5-4 for illustrations of the encoder and front panel assembly. Since these sub-assemblies are an integral part of the A9A1, A9A2 and A9A3 circuit cards (part of front panel assembly) a procedure for disassembly and reassembly of the complete front panel assembly is presented in step-by-step procedures. These procedures permit the removal of any subassembly desired by completing the step-by-step procedures to the point that removes that complete sub-assembly. Inspection, repair and replacement procedures are then presented to properly restore the affected parts. Reassembly instructions provided may then be used to reassembly the front panel assembly.

A. Dismantling and Deassembly

1. Remove top and bottom cover plates from the Receiver by loosening six quarter turn fasteners and disengaging each cover from the slot in the front panel by sliding to the rear.
2. Remove connectors A9A2W1P1 from A6A2 and W13P2, W15P2, W19P1 and W14P2 from the A9A2 circuit card.
3. Remove four 10-32 screws and nylon washers securing the front panel assembly to the gussets of the Receiver and carefully fold the assembly face down.
4. Remove cable W20P1 connector from the A10 module connector A10J2.
5. Remove the 6-32 screw, lock washer and flat washer from encoder disk, remove the disk, then remove spring washer and flat washer under disk.
6. Encoder knob, shaft, retainer ring, shim washer and flat washer can now be removed together from the face of the front panel. Retainer ring should not be removed from groove of shaft unless damaged. Also leave shim washer(s) and flat washer on shaft if they are not damaged. Encoder knob may be removed from shaft by loosening two allen head screws, accessible through holes in circumference of knob.
7. Remove knob from each IF and AF gain control by loosening allen head screw in each knob.
8. Remove twelve 4-40 screws, lock washers and flat washers securing the A9A2 circuit card and carefully lift the circuit card away from the A9A1 circuit card and front panel, making certain that the IF and AF GAIN control and PHONES jack connections are not separated from the A9A2 board. If these three items' connections are to be removed from the circuit card their leads must be unsoldered. The assembly should now appear as in Figure 5-4.
9. Remove 1/2 x 20 hex nut, spring washer, flat washer and nylon washer from encoder spacer-bushing, located on component side of A9A2 circuit card.
10. Remove the twelve threaded standoffs and crinkle washers retaining the A9A1 switch and display circuit card to the front panel. Lift the A9A1 carefully away from the panel. Its full removal will be hindered by the connection of A9A3P1 to the A9A1 card. Remove the tyrap securing the plug and remove the connection. The A9A1 can now be completely removed; take care not to damage the switch and display components mounted to the circuit side of the board.



1. 6-32 Screw
2. Lock Washer
3. Flat Washer
4. Encoder Disk
5. Spring Washer
6. 1/2 x 20 Nut
7. Circuit Card A9A2
8. Front Panel
9. Bushing
10. Retainer Ring
11. Shim Washers
12. Encoder Shaft
13. Encoder Knob
14. Nylon Washer

Figure 5-3. Encoder Assembly, Exploded View

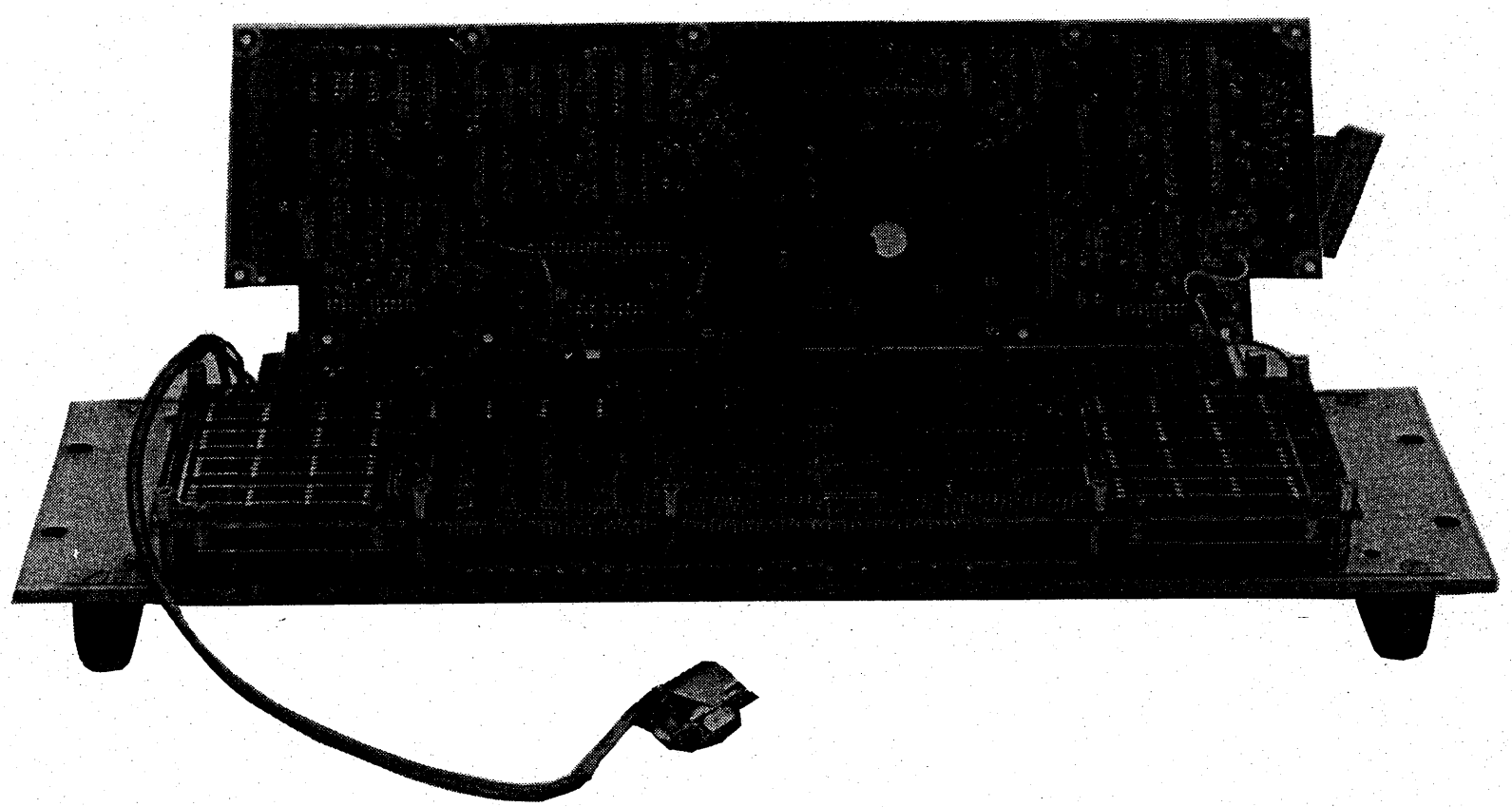


Figure 5-4. Front Panel Assembly, Partially Disassembled

11. From the front of the front panel remove the 1/2 x 20 hex nut, spring washer and flat washer securing the encoder spacer-busing to the front panel and remove the bushing.
12. Remove 3/8 x 32 hex nut, and internal tooth washer from each IF and AF GAIN control and from PHONES jack.
13. From the front panel remove the 1/4 x 24 hex nut, and internal tooth washer securing the POWER-ON switch S1 to the front panel and remove the switch, solder lug and cable assembly W20. NOTE: Cable W20 includes switch S1.
14. Remove four (4) 4-40 hex nuts, lock washers and flat washers from the A9A3 circuit card assembly and remove the assembly.
15. Remove three (3) 4-40 hex nuts, lock washers and flat washers from light diffuser plate and lift the plate away from front panel.

B. Inspection, Repair and or Replacement

1. Encoder Assembly

a. Inspect the encoder spacer-bushing and encoder shaft for excessive wear or damage. Replace both of these items if excessive wear or damage is present.
b. Inspect the flat washers, shim washers, spring washer and nylon washer. Spring washer must be able to take up end play in encoder shaft. Replace broken, damaged or worn items.
c. Inspect the encoder disk for scratches, mars, dents or dirt on the mirrored or black surfaces. Also lay the disk on a flat surface and check for warpage. Replace the disk if it is warped or the mirrored or black surfaces are in any way impaired. Scratches or dark spots on the mirrored surfaces or light spots or scratches on the black areas will affect the encoder operation.
d. Temporarily assemble the retainer ring, flat washer, shim washer, spacer-bushing (shoulder toward disk end of shaft), flat washer, spring washer, disk, flat washer, lock washer and 6-32 screw on the encoder shaft in the order given. Check the end play of the shaft within the spacer-bushing by holding the spacer-bushing and pushing on each end of the shaft. No end play should be detected when pushing on knob end of shaft, but approximately 0.030 inch of end play will be present when the shaft is pushed from the disk end; however, the spring washer should cause the shaft to return to its original position when released. If end play is to great shaft will float in the bushing and either additional or thicker shim washer must be added. If end play is insufficient shaft will not spin freely in bushing, and less shim is required. Disassemble the unit when correct end play is obtained.
e. Inspect the encoder knob for damage; replace if necessary.

2. Controls, POWER-ON Switch and PHONES Jack

a. Check the IF and AF GAIN controls for freedom of operation, signs of excessive heat or other damage. Using an ohmmeter check the resistance of each control. The IF GAIN control (R1) should be 50K ohms $\pm$10%. The AF GAIN control (R2) should be 25K ohms $\pm$10%. Replace either or both controls if they are found to be sub-standard.
b. Inspect the AF and IF GAIN control knobs for any signs of damage; replace as required.

c. Inspect the PHONES Jack for excessive wear or damage; replace if necessary.
d. Inspect the POWER-ON switch for freedom of operation, signs of arcing or other damage, replace if necessary.

3. Edge Lighting Assembly A9A3

a. Visually inspect the assembly for any signs of damage. Also inspect the lead wires and connector W1P1. The assembly is non-repairable and must be replaced if damage has occurred.
b. Connect a 15 volt supply through connector W1P1 to the edge lighting. All LED's should illuminate. If any LED's do not illuminate, replace the assembly.

4. Circuit Card Assembly A9A1

a. Check components for excessive heat, loose connections, corroded leads, and other damage.
b. Check LCDs for looseness or damage to the units.
c. Check connectors for damaged or bent pins, loose connections, corrosion or other damage.
d. Check the circuit card for damaged tracks, excessive heat, corrosion or other signs of deterioration.
e. Check individual switches for smooth operation and button caps for damage.

C. Reassembly

1. Install light diffuser over studs in front panel so that windows match the opening in front panel. Install four (4) 4-40 hex nuts, lock washers and flat washers.
2. Install the edge lighting assembly over the studs so that its windows fit the front panel openings. Install four (4) 4-40 hex nuts, lock washers and flat washers.
3. If cable W20 has been removed from front panel. Replace as follows: Install solder lug over shank of switch, then install shank through 1/4 inch round hole in left side of front panel. Be sure switch is placed so that ON is toward top of panel. Secure with internal tooth washer and 1/4 x 24 hex nut.
4. Install the shoulderless end (shoulder toward circuit card A9A2) of the encoder spacer-bushing through the 1/2 inch round hole located near the center of the front panel. Secure with flat washer, spring washer and 1/2 x 20 hex nut.
5. If AF or IF GAIN control or PHONES jack leads have been unsoldered they must be resoldered. Refer to Figure 5-3 for proper lead identification. Insert the shaft of these three items into their respective holes in the front panel and place circuit card A9A1 on the standoffs extending from the back of the front panel. Connect A9A3W1P1 to A9A1J8 and secure. Be sure encoder spacer-bushing is fitted through hole in circuit card. Secure the circuit card with twelve (12) standoffs and crinkle washers.
6. Secure the IF and AF GAIN controls and PHONES jack each with an internal tooth washer and 3/8 x 32 hex nut.

7. Install the IF and AF GAIN control knobs and secure them by tightening the allen head screw in each knob.
8. Lower the A9A2 circuit card assembly on to the standoffs holding A9A1. Take care to align the connectors between the two cards before pressing the boards firmly together. Secure using the twelve (12) 4-40 screws, lock and flat washers. Press the leads between A9A2 and the front panel controls into the cutouts provided on the lower edge of the A9A1 circuit card.
9. Place the 1/2 inch nylon washer, flat washer and spring washer over the threads of the spacer-bushing in the order given and secure them with the 1/2 x 20 hex nut. Tighten only finger tight.
10. Assembly the retainer ring, flat washer and shim washer on the encoder shaft, in the order given. Install the encoder shaft, from the front of the front panel, through the spacer-bushing. Install flat washer, spring washer, disk (mirror surfaces toward A9A2 circuit card), flat washer and lock washer in the order given. Secure with 6-32 screw.
11. Install the encoder knob and secure by tightening two allen head screws in the knob. Inspect the encoder assembly for freedom to spin and for wobble in the disk.
12. Install the ribbon cables into their respective connectors P2 and P3 located on the A9A2 circuit card. Take care to note the correct polarization.
13. Connect connectors W14P2, W19P1, W15P2 and W13P2 to their respective connectors on the A9 circuit card. Connect connector A2W1P1 to its connector on the A6A2 circuit card, connect cable W20P1 connector to A10J2 on the A10 module.
14. Install the front panel assembly to the gussets of the Receiver with four nylon washers and 10-32 screws.
15. Install the top and bottom cover plates on the Receiver and secure each cover with six quarter turn fasteners.

SECTION VI
REPLACEMENT PARTS LIST

6.1 INTRODUCTION

This section contains a complete listing of all replaceable parts contained in RA6793A Receiver. The parts list tables are arranged in sequence by unit designation.

Since electromechanical equipment undergoes periodic changes over time, due to factors such as operational time, environmental conditions, etc., degradation of individual subassemblies and parts occur. Replacement Parts Lists act as reference guides for users and must be consulted to identify and locate parts. To be able to identify and locate parts the user must be familiar with the unit designation method, reference designator prefixes, illustrations and schematics. This method is composed of assigning a class letter such as R for resistor or C for capacitor followed by an identifying number -1, -2, -3, -4, etc.

This partial reference designation must be further identified by including a reference designator prefix, such as A1A6, which classes the item by assembly (A1) and subassembly (A6). The composite alphanumeric code then becomes the complete reference designation. For example A4C1 would be identified as the first (1) capacitor (C) of the fourth (4) assembly (A).

A detail part of subassembly A1A6 such as a resistor of capacitor would be numbered R1 or C1, resulting in a full reference designation number of A1A6C1.

If components on an assembly, module or subassembly need to be replaced, the following parts list information will provide the user with the proper ordering information. Pictures of assemblies and subasemblies along with component location diagrams are shown for ease of physically locating the desired components.

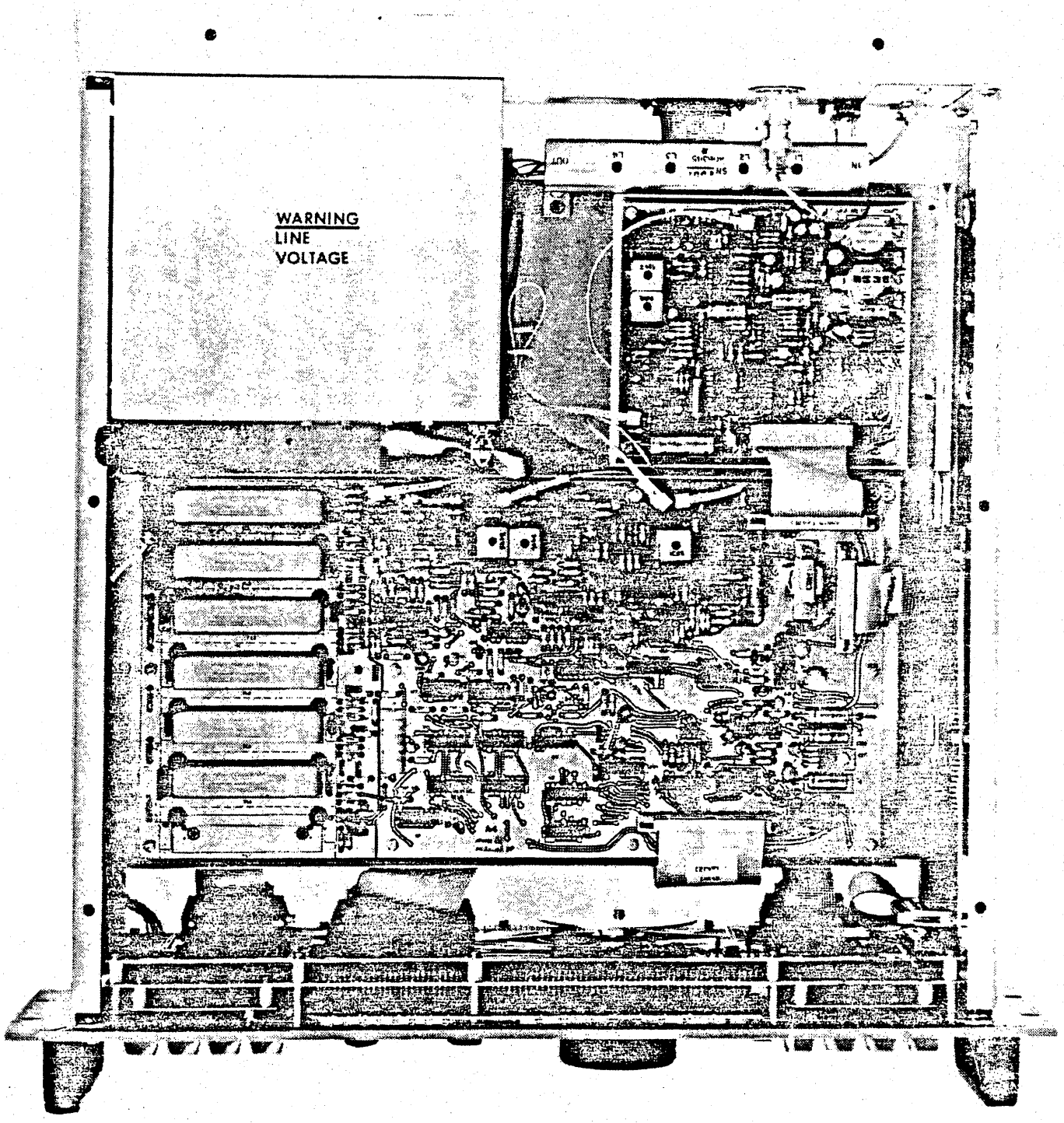


Figure 6-1. RA6793A HF Receiver, Top View

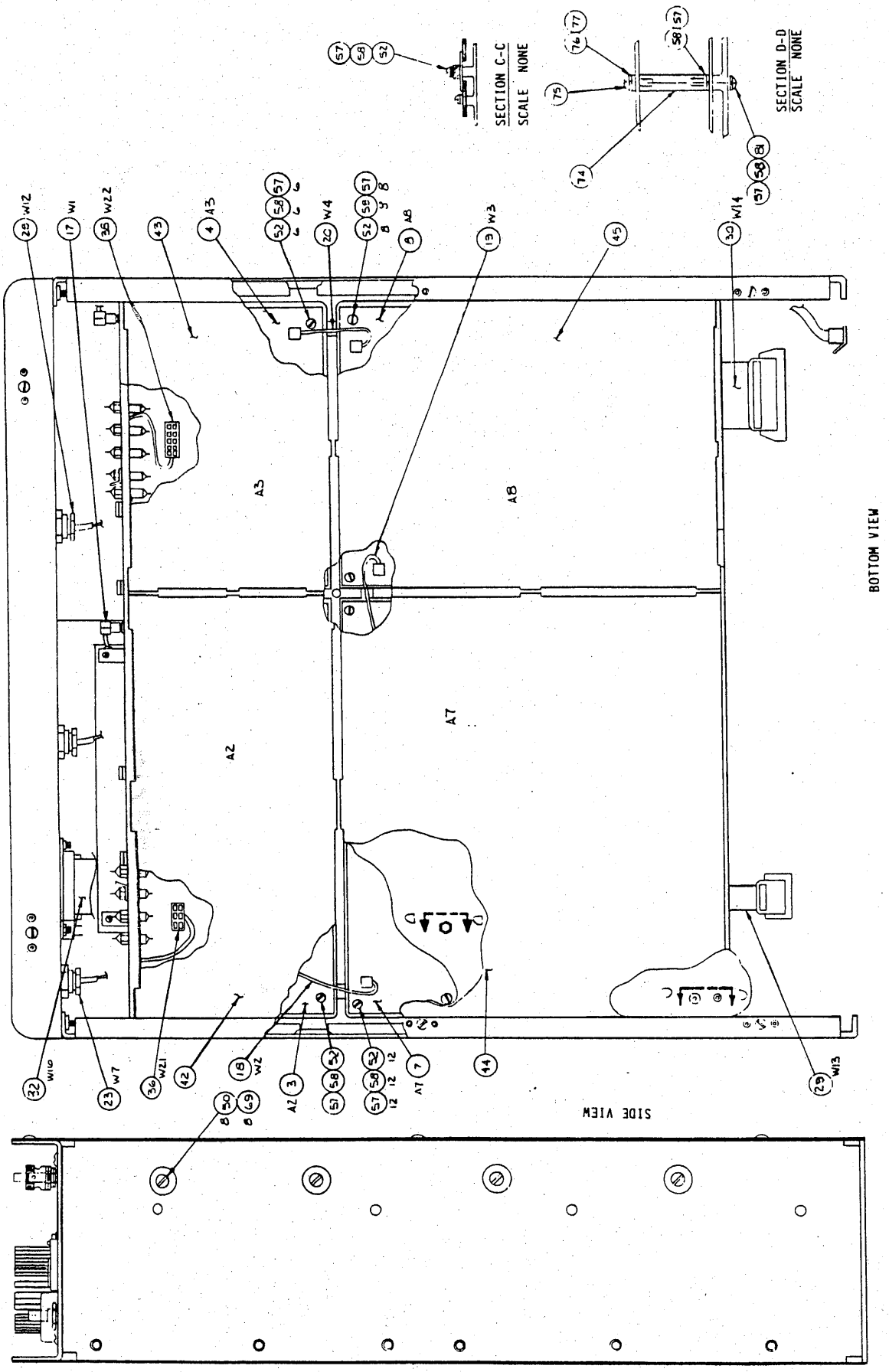


Figure 6-2. RA6793A HF Receiver, Bottom View

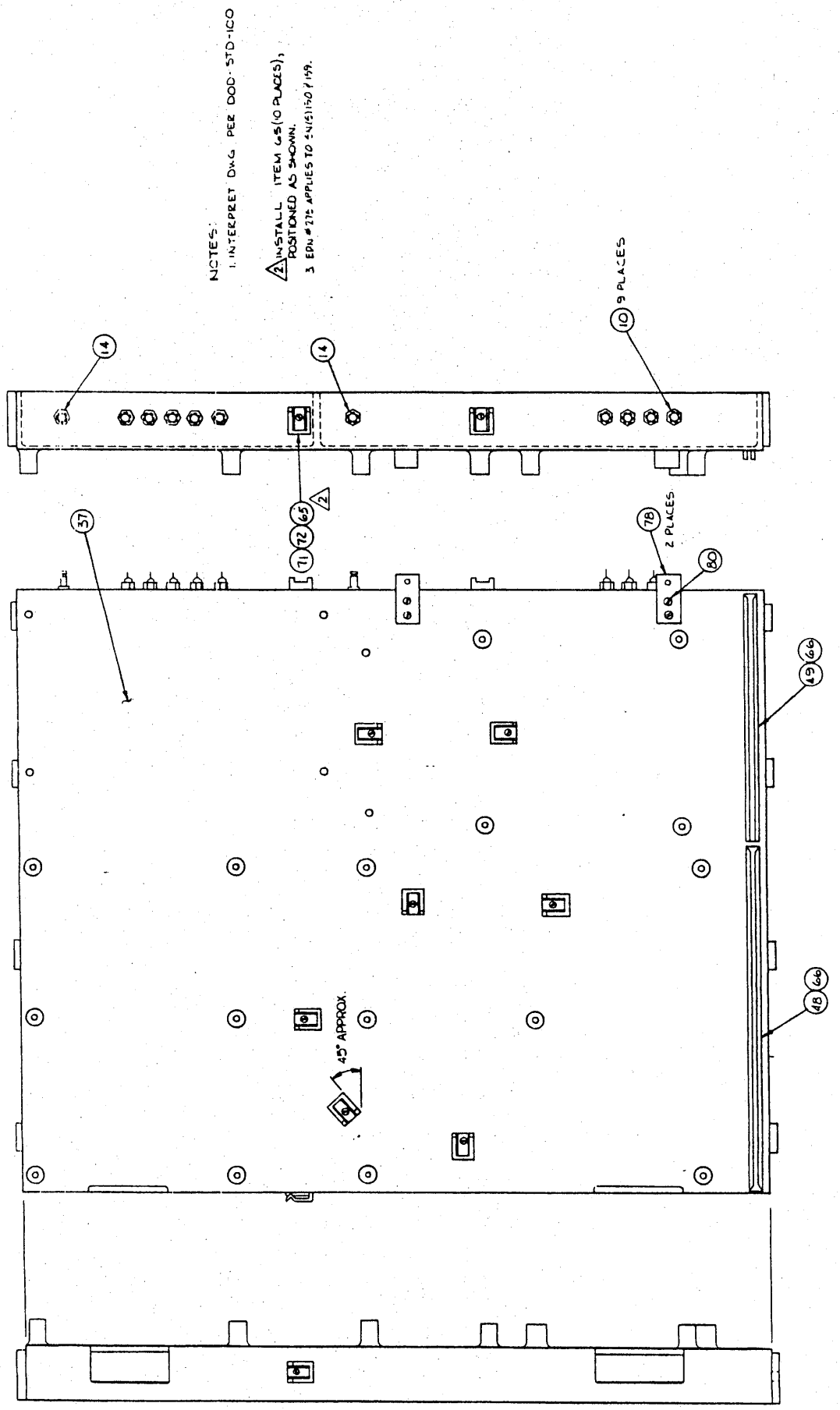


Figure 6-3. Location of Modules, Top View

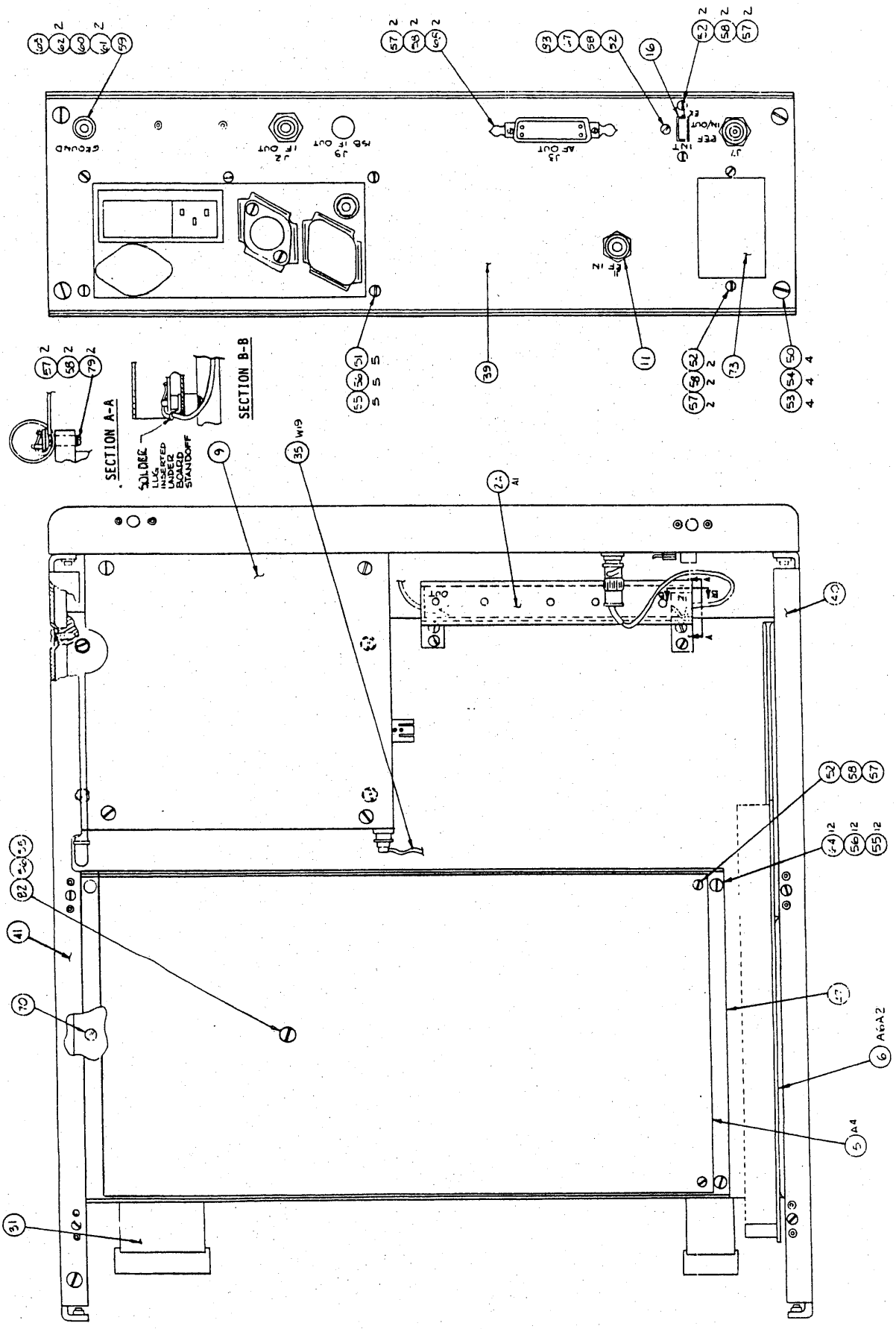


Figure 6-4. RA6793A HF Receiver, Chassis Mechanical Parts

Table 6-1. Main Chassis Assembly
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
		Main Chassis Assembly (Inteconnecting Wiring Diagram 5200002)	4100101-501	1
2	A1	· RF Low Pass Filter Module Assembly	A09691	1
	A1A1	. . RF Low Pass Filter Circuit Card Assembly (Schematic No. 09933)	A09932	1
3	A2	· 1st Mixer Circuit Card Assembly (Schematic No. 09018)	A08966-2	1
4	A3	· 2nd Mixer Circuit Card Assembly (Schematic No. 08162)	A08191	1
5	A4	· Main IF/AF Converter Circuit Card Assembly (Schematic No. 09664)	A09663	1
	A5	· · ISB Demodulator Module Assembly (Option)		
	A6	. Microcomputer Control Assembly	A08979	1
	A6A1	. . Remote Control Interface Circuit Card Assembly (Option)		
6	A6A2	· · Microprocessor Circuit Card Assembly (Schematic No. 420018)	4100030	1
		· · · Romset, RA9303	1600002	1
7	A7	· 1st LO Synthesizer Circuit Card Assembly (Schematic No. 09256)	A09134	1
8	A8	· 2nd LO/BFO Synthesizer Circuit Card Assembly (Schematic No. 09633)	A09632	1
9	A10	· Power Supply Module Assembly (Schematic No. 08512)	A08389	1
10	C1-C9	· Capacitor, Feed-thru, .001 μf, $\pm$20%	26406	9
11	J1	· Connector, N-BNC Bulkhead, UG606/U (RF IN)	60063	1

Table 6-1. Main Chassis Assembly Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
12	J2	• Connector, BNC Bulkhead p/o W12, IF OUT	60046	1
13	J3	• Connector, "D" Subminiature, 25-Pin p/o W16, (AF OUT)	61248	1
	J4	• Not Used		
15	J5-J6	• Connector, SMB-SMB, Bulkhead	60057	2
	J7	• Connector, BNC Bulkhead, p/o W7 (REF IN/OUT)	60046	1
	J9	• Connector, BNC Bulkhead ISB IF OUT (optional)	60046	1
	S1	• Not Used		
16	S2	• Switch, Slide DPDT, Reference Frequency Input/Output (INT-EXT)	52425	1
17	W1	• Cable Assembly, RF Coax, 2nd IF Signal (A3 to A4)	B08555-1	1
18	W2	• Cable Assembly, RF Coax, 1st LO Signal (A7 to A2)	B08555-2	1
19	W3	• Cable Assembly, RF Coax, Frequency Reference (A7 to A8)	B08555-3	1
20	W4	• Cable Assembly, RF Coax, 2nd LO Signal (A8 to A3)	B08555-4	1
	W5	• Not Used		
22	W6	• Cable Assembly, RF Coax, BFO Signal (A8 to A4)	B08555-5	1
23	W7	• Cable Assembly, RF Coax, Frequency Reference Input/Output (A8 to J7 on rear panel)	B08556-1	1
	W8-W11	• Not Used		
28	W12	• Cable Assembly, RF Coax, Main IF Signal (A4 to J2 on rear panel)	B08556-2	1
29	W13	• Cable Assembly, Control, 1st LO Synthesizer (A7 to A9)	B08376	1

Table 6-1. Main Chassis Assembly
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
30	W14	· Cable Assembly, Control, 2nd LO/BFO Synthesizer (A8 to A9)	B08558	1
31	W15	· Cable Assembly, Control, Main IF/AF (A4 to A9)	C08563	1
32	W16	· Cable Assembly, Main Audio Output (A4 to J3 on rear panel)	C08568	1
	W17	· Not Used		
	W18	· Cable Assembly, AC Power Input	57035	1
35	W19	· Cable Assembly, DC Power Supply (A10 to A9)	D08569	1
	W20	· Cable Assembly, AC Line Switching	B08670	1
36	W21	· Cable Assembly, DC Power Supply (A10 to A2)	B08561	1
38	W22	· Cable Assembly, DC Power Supply (A10 to A3)	B08560	1
39		· Rear Panel	D08936	1
40		· Gusset, Right Side Panel	D08468	1
41		· Gusset, Left Side Panel	D08469	1
41		· Cover, 1st Mixer Circuit Card Assembly	C08665	1
43		· Cover, 2nd Mixer Circuit Card Assembly	C08666	1
44		· Cover, 1st LO Synthesizer Circuit Card Assembly	C08667	1
45		· Cover, 2nd LO/BFO Synthesizer	C08668	1
		· Bracket, Filter Support, Main IF/AF Circuit Card Assembly	D08496	1

Table 6-1. Main Chassis Assembly
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
		· Base Plate, Main IF/AF Circuit Card Assembly	D08497	1
48		· Slide, Circuit Card Assembly	81795	1
49		· Slide, Circuit Card Assembly (Modified)	C08562	1
50		· Screw, Pan Head #8-32 x 3/8" Lg.	76042	12
51		· Screw, Pan Head #6-32 x 3/8" Lg.	76027	15
52		· Screw, Pan Head #4-40 x 5/16" Lg.	76013	44
53		· Washer, Flat #8	75026	4
54		· Washer, Split Lock #8	75004	4
55		· Washer, Flat #6	75024	17
56		· Washer, Split Lock #6	75003	17
57		· Washer, Flat #4	75022	52
58		· Washer, Split Lock #4	75002	52
59		· Screw, Pan Head #10-32 x 3/4" Lg.	76264	1
60		· Nut, #10-32 Hex	75210	1
61		· Washer, Flat #10	75027	2
62		· Washer, Split Lock #10	75005	2
63		· Nut, Knurled #10-32	75448	1
64		· Screw, Pan Head #6-32 x 5/16" Lg.	76026	11
65		· Clamp, Cable	81267	10
67		· Nut, #4-40	75203	4
68		· Latch Assembly, Spring	61188	2
69		· Washer, #8 Spring	75121	8
70		· Screw, Flat Head #6-32 x 3/8" Lg.	76535	1
71		· Screw, Flat Head #4-40 x 1/4" Lg.	76520	10
73		· Plate, Blanking (Ref. A6A1)	B08492	1
74		· Standoff, Insulated	B08648	1
75		· Screw, Pan Head #2-56 x 1/4" Lg.	76002	1
76		· Washer, Split Lock #2	75001	1

Table 6-1. Main Chassis Assembly Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
77		• Washer, Flat #2	75021	1
78		• Block, Mounting	A08656	2
79		• Screw, Pan Head #4-40 x 3/4" Lg.	76018	2
80		• Screw, Flat Heat #6-32 x 1/2" Lg.	76421	4
81		• Screw, Pan Head #4-40 x 11/16" Lg.	79095	1
82		• Screw, Pan Head #6-32 x 1 1/8" Lg.	79099	1
83		• Lug, #4	70007	1
		• Covers, Top and Bottom	81958	1
		• Dust Cap (Ref. J1)	81958	1
		• Dust Cap (Ref. J2, J7)	81959	2
		• Screw #2 x 1/8"	79067	2
		• Shell, DB51272-1 (Ref. J3)		1
		• Latch, D110278 (Ref. J3)	61187	1

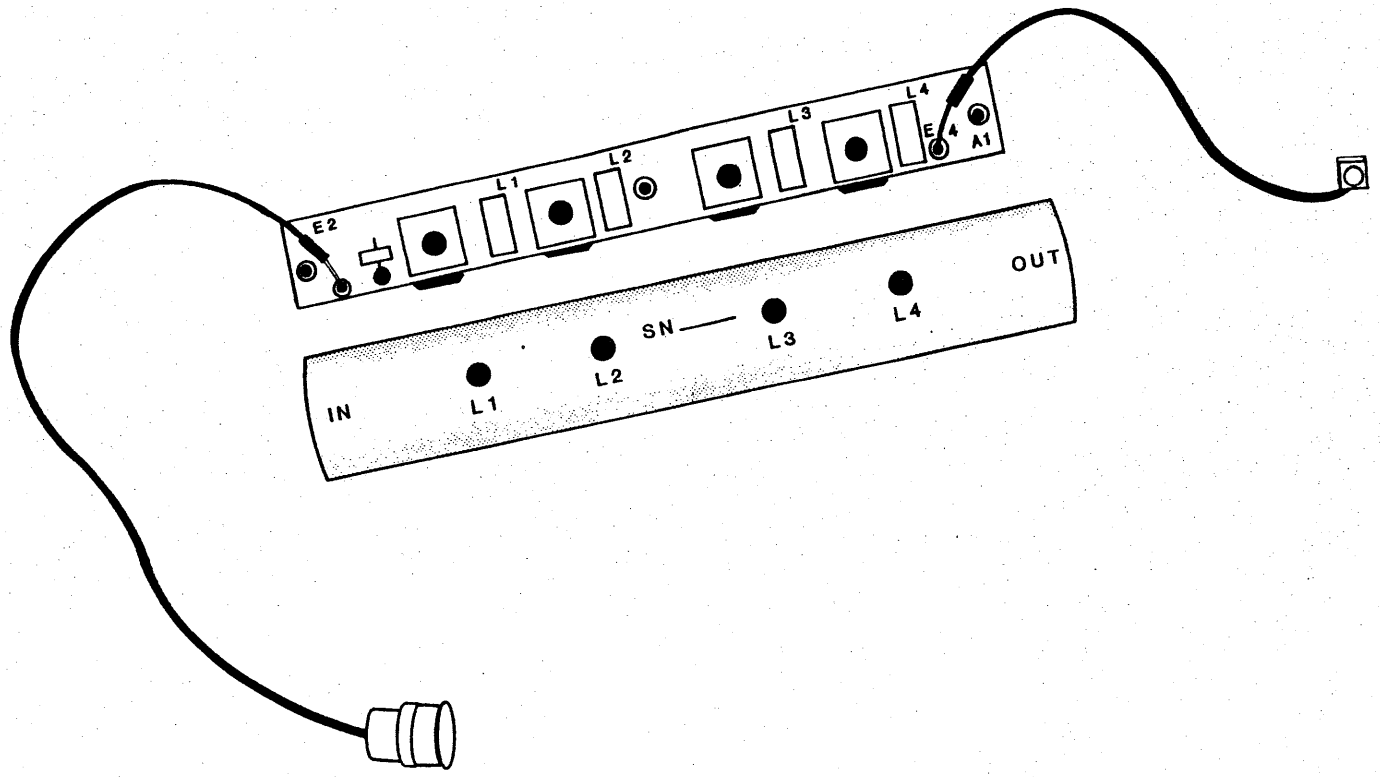


Figure 6-5. Low Pass Filter Circuit Card Assembly (A1)

Table 6-2. RF Low Pass Filter Module Assembly (A1)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A1	RF Low Pass Module Assembly	A09691	1
	A1A1	· RF Low Pass Filter Circuit Card Assembly (See Table 6-3 for further breakdown)	A09932	1
		· Module Cover		1

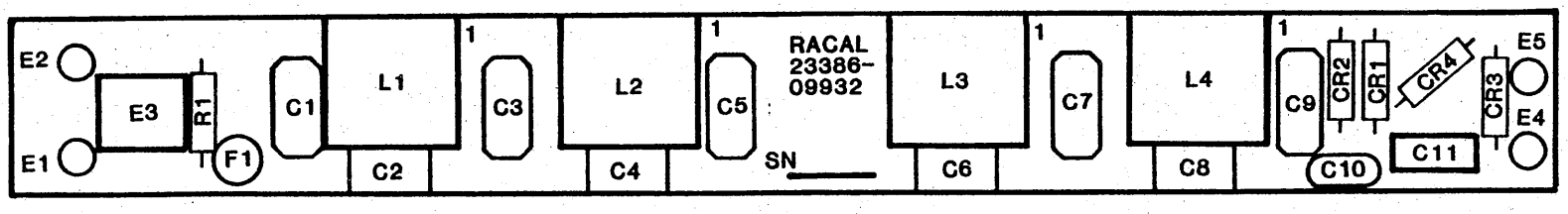


Figure 6-6. RF Low Pass Filter Circuit Card Assembly (A1A1)
Component Location Diagram

Table 6-3. RF Low Pass Filter Circuit Card Assembly (A1A1)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A1A1	RF Low Pass Filter Circuit Card Assembly (Schematic No. 09933)	A09932	1
		· Printed Circuit Card Wiring Assembly	09934	1
	C1, C5	· · Capacitor, Mica, 110 pf, ±2%, CM05	22139	2
	C2	· · Capacitor, Mica, 10 pf, ±1/2 pf, CM05	22161	1
	C3	· · Capacitor, Mica, 150 pf, ±2%, CM05	22101	1
	C4	· · Capacitor, Mica, 75 pf, ±5%, CM05	22020	1
	C6	· · Capacitor, Mica, 91 pf, ±2%, CM05	22123	1
	C7	· · Capacitor, Mica, 120 pf, ±2%, CM05	22113	1
	C8	· · Capacitor, Mica, 43 pf, ±2%, CM05	22137	1
	C9	· · Capacitor, Mica, 82 pf, ±2%, CM05	22108	1
	C10	· · Capacitor, Ceramic, .01 µf	21791	1
	C11	· · Ceramic, 0.47 µf, 100 V	21790	1
	CR1, CR3	· · Diode, 1N916	35514	1
	CR2, CR4	· · Diode, Zener, 1N4729A	33560-3V6	2
	E1, E2 E4, E5	· · Terminal	70028	4
	E3	· · Arrestor, Lighting	64001	1
	F1	· · Fuse, Littlefuse, #273-500	40010	1
	L1	· · Coil, RF Variable	08477-1	1
	L2	· · Coil, RF Variable	08477-2	1
	L3	· · Coil, RF Variable	08477-3	1
	L4	· · Coil, RF Variable	08477-4	1
	R1	· · Resistor, Film, 10 K, 1/4 W, ±2%	12161-103	1
	W1	· · Cable Assembly	09617	1
	W2	· · Cable Assembly	08479-4	1
		· · Spacer, 4-40 x 3/16 Lg.*	SP02-009	3

*NOTE: This component is not shown on illustration.

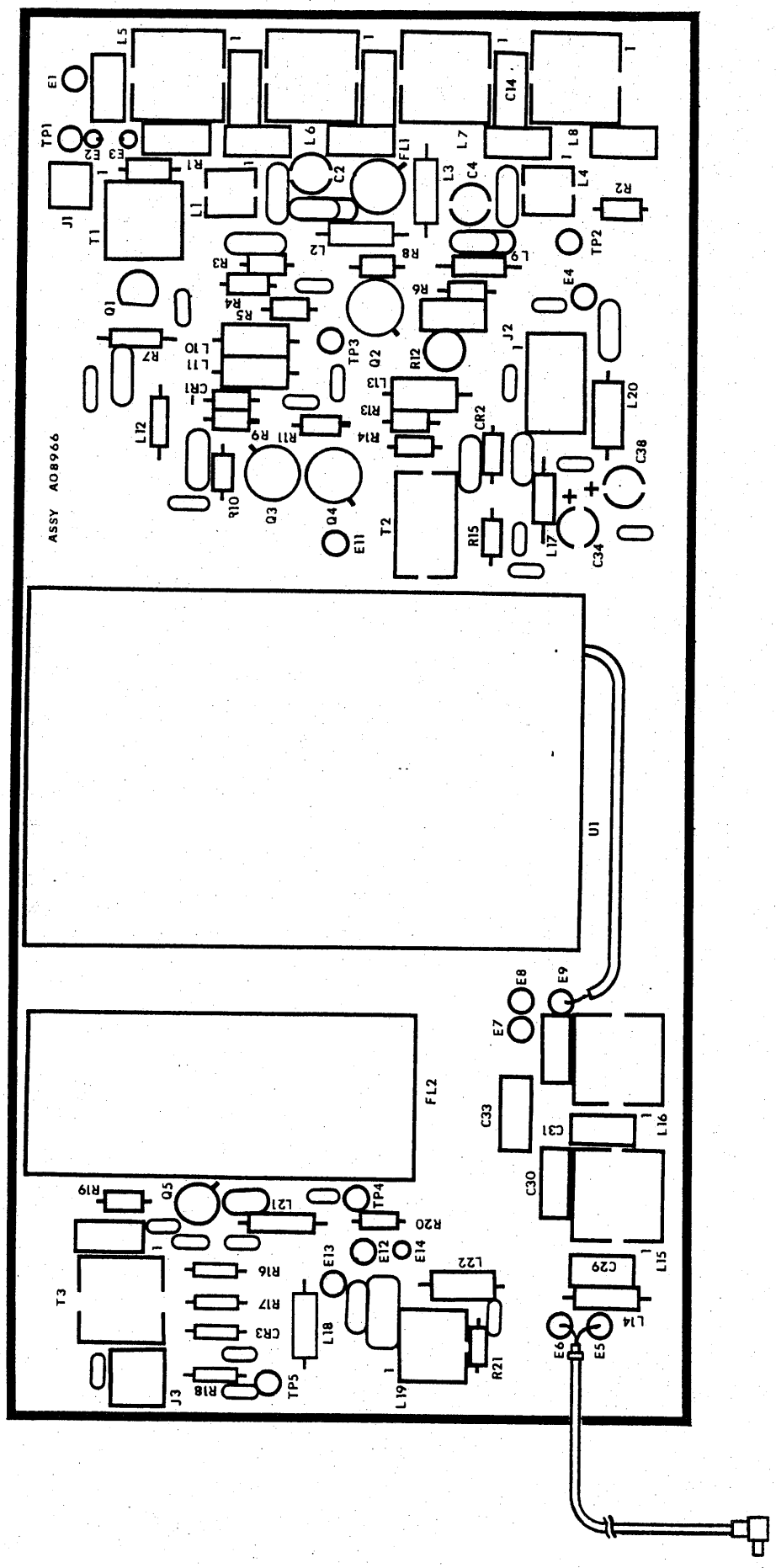


Figure 6-7. 1st Mixer Circuit Card Assembly (A2)
Component Location

Table 6-4. 1st Mixer Circuit Card Assembly (A2)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A2	1st Mixer Circuit Card Assembly (Schematic No. 09018)	A08966-2	1
		· Printed Circuit Card Assembly	D08964	1
	C1-C6	· · Not Used		
	C7, C8	· · Capacitor, Mica, 82 pf, ±2%	22108	2
	C9	· · Capacitor, Mica, 270 pf, ±2%	22103	1
	C10, C11	· · Capacitor, Mica, 150 pf, ±2%	22101	2
	C12	· · Capacitor, Mica, 18 pf, ±2%	22129	1
	C13	· · Capacitor, Mica, 10 pf, ±1/2 pf	22161	1
	C14	· · Capacitor, Mica, 30 pf, ±2%	22160	1
	C15	· · Capacitor, Mica, 240 pf, ±5%	22032	1
	C16, C18, C20, C25, C26, C35, C37, C39, C45, C51, C52	· · Capacitor, Ceramic, .01 µf, ±20%	21733	11
	C17, C19, C22, C36, C40, C50	· · Capacitor, Ceramic, 0.1 µf, ±20%	21732	6
	C21, C46, C48	· · Not Used		
	C23, C27, C41, C43, C44, C49, C53	· · Capacitor, Ceramic, .001 µf, ±20%	21756	7
	C24, C28	· · Capacitor, Ceramic, 1 µf, ±20%	21748	2
	C29, C31	· · Capacitor, Mica, 100 pf, ±2%	22109	2
	C30	· · Capacitor, Mica, 91 pf, ±2%	22123	1
	C32	· · Capacitor, Mica, 43 pf, ±2%	22137	1
	C33	· · Capacitor, Mica, 68 pf, ±2%	22107	1
	C34, C38	· · Capacitor, Tantalum, 15 µf	25062-156	2
	C42	· · Capacitor, Mica, 33 pf, ±2%	22106	1

Table 6-4. 1st Mixer Circuit Card Assembly (A2)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	C47	· · Capacitor, Mica, 27 pf, 2%	22008	1
	CR1, CR2	· · Diode, 1N916	35514	2
	CR3	· · Diode, KS8379	35557	1
	FL1	· · Not Used		
	FL2	· · Filter, 40.455 MHz	08404	1
	J1, J3	· · Connector, SMB	60044	2
	J2	· · Connector, Control	08499-4	2
	L1, L4	· · Not Used		
	L2, L3			
	L5	· · Coil Assembly, RF Variable	08500-1	1
	L6	· · Coil Assembly, RF Variable	08500-2	1
	L7	· · Coil Assembly, RF Variable	08500-3	1
	L8	· · Coil Assembly, RF Variable	08500-4	1
	L9, L11,	· · Choke, RF, 10 µH	43029	5
	L12, L13,			
	L17			
	L10	· · Choke, RF, 2.2 µH	43025	1
	L14	· · Choke, RF, 0.27 µH	43051	1
	L15	· · Coil Assembly, RF Variable	08477-6	1
	L16	· · Coil Assembly, RF Variable	08477-7	1
	L18	· · Choke, RF, 1 µH	43024	1
	L22	· · Choke, RF, 0.56 µH	43052	1
	L19	· · Not Used		
	L20, L21	· · Choke, RF, 15 µH	43030	2
	Q1	· · Transistor, 2N4126	31508	1
	Q2, Q4	· · Transistor, 2N3866	32019	2
	Q3	· · Transistor, 2N5160	32027	1
	Q5	· · Transistor, U310	32507	1
	R1, R2	· · Not Used		
	R3, R8,	· · Resistor, Film, 1 K, 2%, 1/4 W	12161-102	3
	R18			
	R4	· · Resistor, Film, 5.6 K, 2%, 1/4 W	12161-562	1

Table 6-4. 1st Mixer Circuit Card Assembly (A2)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R5	· · Resistor, Film, 2.2 K, 2%, 1/4 W	12161-222	1
	R6	· · Resistor, Film, 47 ohm, 2%, 1/4 W	12161-470	1
	R7	· · Resistor, Composition, 15 ohm, ±5%, RC20, 1/2 W	10919	1
	R9, R15, R16, R21	· · Resistor, Film, 220 ohm, 2%, 1/4 W	12161-221	4
	R10, R14, R19	· · Resistor, Film, 10 ohm, 2%, 1/4 W	12161-100	3
	R11, R13	· · Resistor, Film, 1.2 K, 2%, 1/4 W	12161-122	2
	R12	· · Resistor, Trimmer, 5 K	16090-502	1
	R17	· · Resistor, Film, 10 K, 2%, 1/4 W	12161-103	1
	R20	· · Resistor, Film, 100 ohm, 2%, 1/4 W	12161-101	1
	T1	· · Not Used	09241	1
	T2	· · Transformer, RF Wideband	08501	1
	T3	· · Transformer, RF Variable	08503	1
	U1	· · Mixer Box Assembly	08923-2	1
	W1	· · Cable Assembly, Coax	08479-1	1
		· · Transistor Pad (Ref. Q2, Q3, Q4, FL1)*	70750	4
		· · Heat Sink (Ref. Q2)*	70790	1
		· · Heat Sink (Ref. Q3, Q4)*	70784	2
		· · Heat Sink Plate (Ref. Q3, Q4)*	B09226	1
		· · Lug, Ground, #4*	70007	1
		· · Nut, Hex, #4-40*	75203	2
		· · Screw, Pan Head #4-40 x 3/16 Lg.*	76011	2
		· · Screw, Pan Head #4-40 x 7/16 Lg.*	76015	4
		· · Transistor Pad (Ref. Q5)*	70752	1
		· · Washer, Split Lock #4*	75002	8
		· · Washer, Flat #4*	75022	8
		· · Wire, Buss, #24*	58007	1

*NOTE: These components are not shown on illustration.

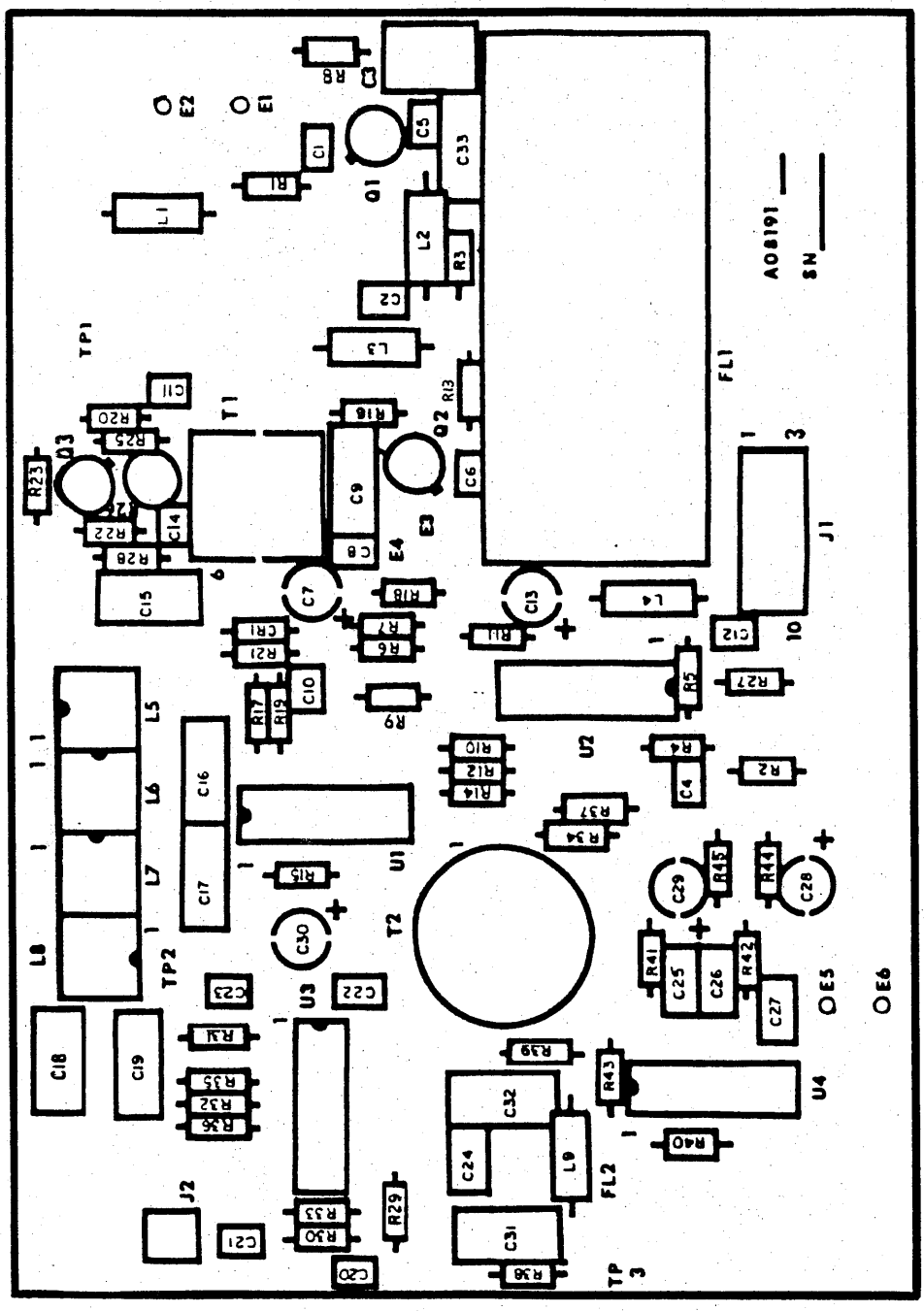


Figure 6-8. 2nd Mixer Circuit Card Assembly (A3)
Component Location

Table 6-5. 2nd Mixer Circuit Card Assembly (A3)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A3	2nd Mixer, Circuit Card Assembly	08191	1
	C1, C2, C5, C6, C8, C10, C11, C12, C14, C20, C21, C22, C23	· Capacitor, Ceramic, 1000 pf,	21756	13
	C3	· Capacitor, Variable, 5-50 pf (Johanson)	28037	1
	C4	· Capacitor, Ceramic, 0.01 µf, 50 V, ±20%	21733	1
	C7, C30	· Capacitor, Tantalum, 1 µf, 35 V, ±20%	25060-105	2
	C9	· Capacitor, Mica, 33 pf, 50 V, ±2%	22106	1
	C13, C28, C29	· Capacitor, Tantalum, 15 µf, 20 V, ±20%	25062-156	3
	C15, C16 C17	· Capacitor, Mica, 68 pf, 500 V, ±2%	22107	3
	C18	· Capacitor, Mica, 82 pf, 500 V, ±2%	22108	1
	C19	· Capacitor, Mica, 330 pf, 500 V, ±2%	22117	1
	C24-C27	· Capacitor, Ceramic, 0.1 µf, 500 V, ±20%	21732	4
	C31, C2	· Capacitor, Mica, 22 pf, 500 V, ±2%	22171	2
	C33	· Capacitor, Mica, 15 pf, 500 V, ±2%	22116	1
	CR1	· Diode, Pin (Motorola)	35557	1
	FL1	· Filter, 40.455 MHz	08576	1
	J1	· Connector, RF, IN	08499-5	1
	J2	· Connector, RF, SMB	60044	1
	L1, L3 L9	· Choke, RF, 15 µH, ±10%	43030	3
	L2	· Choke, RF, 0.56 µH	43052	1
	L4	· Choke, RF, 100 µH, ±5%	43033	1

Table 6-5. 2nd Mixer Circuit Card Assembly (A3)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	L5-L8	· Coil, RF, Variable	08522	1
	Q1, Q2	· Transistor, Field Effect	32507	1
	Q3	· Transistor, NPN	31500	1
	R1, R10, R13, R18	· Resistor, Film, 220 ohms, ±2%, 1/4 W	12161-221	4
	R2, R3, R20, R21, R27, R35	· Resistor, Film, 100 ohms, ±2%, 1/4 W	12161-101	6
	R4	· Resistor, Film, 220 K, 2%, 1/4 W	12161-224	1
	R5, R6, R11	· Resistor, Film, 220 K, ±2%, 1/4 W	12161-223	3
	R7, R23	· Resistor, Film, 4.7 K, ±2%, 1/4 W	12161-472	1
	R8, R12, R28	· Resistor, Film, 2.2 K, ±2%, 1/4 W	12161-222	3
	R9	· Resistor, Film, 100 K, ±2%, 1/4 W	12161-104	1
	R14	· Resistor, Film, 27 ohms, ±2%, 1/4 W	12161-270	1
	R15	· Resistor, Film, 560 ohms, ±2%, 1/4 W	12161-561	1
	R16, R37	· Resistor, Film, 10 ohms, ±2%, 1/4 W	12161-100	2
	R17, R36	· Resistor, Film, 10 K, ±2%, 1/4 W	12161-103	2
	R19, R29, R33	· Resistor, Film, 1 K, ±2%, 1/4 W	12161-102	3
	R22	· Resistor, Film, 39 K, ±2%	12161-393	1
	R24	· Not Used		
	R25	· Resistor, Film, 56 ohms, ±2%, 1/4 W	12161-560	1
	R26	· Resistor, Trimmer, 500 ohms, ±20%	16090-501	1
	R30, R31, R32, R40, R44, R45	· Resistor, Film, 47 ohms, ±2%, 1/4 W	12161-470	6
	R34	· Resistor, Film, 39 ohms, ±2%, 1/4 W	12161-390	1
	R38, R39	· Resistor, Fil, 1.2 K, ±2%, 1/4 W	12161-122	2

Table 6-5. 2nd Mixer Circuit Card Assembly (A3)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R41, R42	· Resistor, Film, 330 ohms, ±2%, 1/4 W	12161-331	1
	R43	· Resistor, Film, 1.5 K, ±2%, 1/4 W	12161-152	1
	T1	· Transformer, RF, Variable	08503	1
	T2	· Transformer Assembly	08530	1
	U1	· Integrated Circuit, Transistor Array	36785	1
	U2	· Integrated Circuit, Quad Op-Amp	36784	1
	U3	· Integrated Circuit, 2nd Mixer	36748	1
	U4	· Integrated Circuit, Op-Amp	36747	1
	W1	· Cable, 40.455 MHz Input	08479-2	1
	W2	· Cable, 455 kHz Output	08479-3	
		· Transistor Pad, Ref. Q1, Q2 and Q3	70752	1

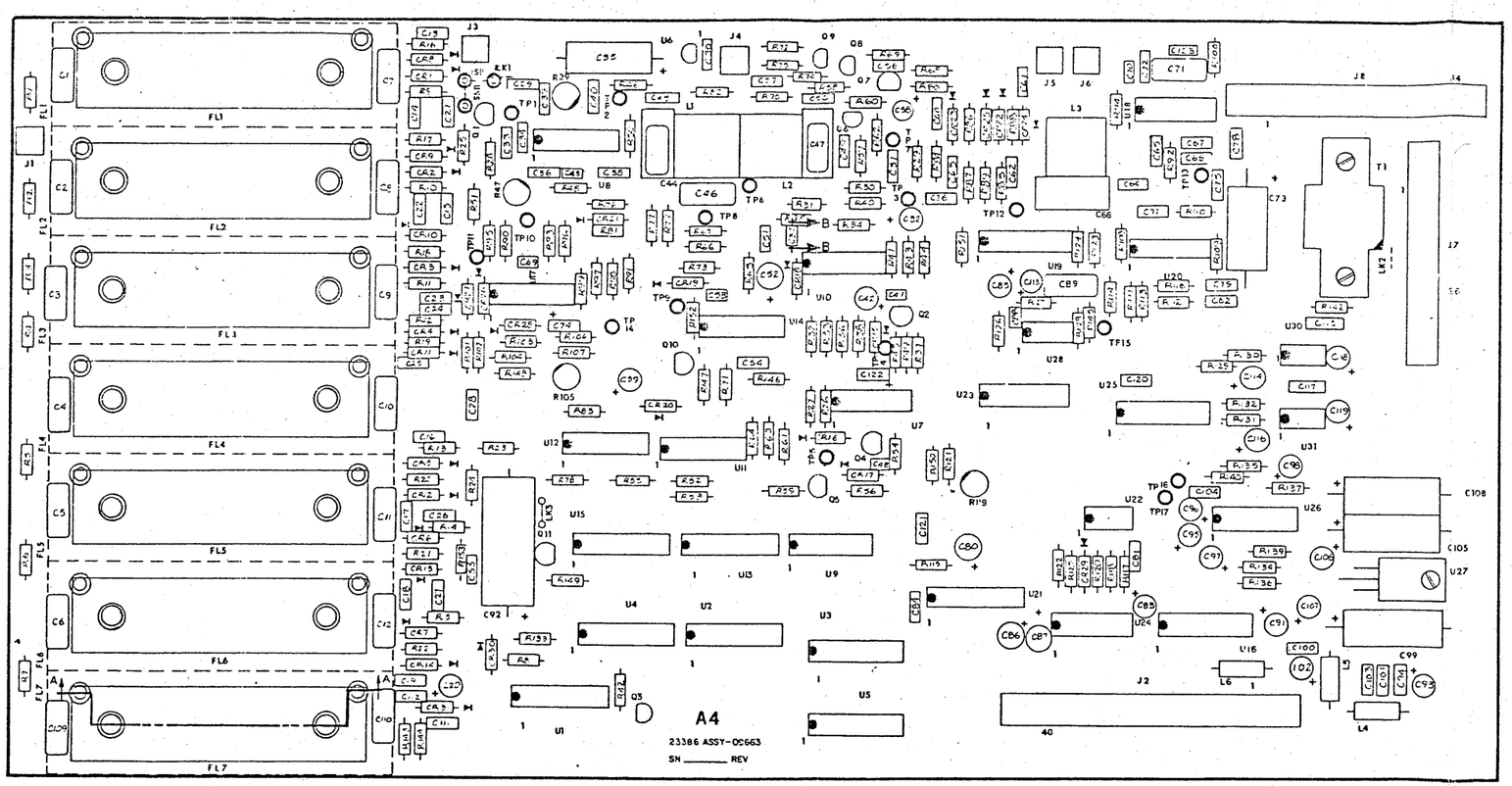


Figure 6-9. Main IF/AF Circuit Card Assembly (A4) Component Location Diagram (09663)

Table 6-6. Main IF/AF Circuit Card Assembly (A4)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A4	Main IF/AF Converter Circuit Card Assembly (Schematic No. 09664)	A09663	1
		· Printed Circuit Card Wiring Assembly	E09665	1
	C1, C2	· · Capacitor, Mica, 270 pf	22372-271	1
	C3	· · Capacitor, Mica, 180 pf	22372-181	1
	C4	· · Capacitor, Mica, 110 pf	22372-111	1
	C5	· · Capacitor, Mica, 360 pf	22372-361	1
	C6	· · Capacitor, Mica, 750 pf	07883-4	1
	C7, C8	· · Capacitor, Mica, 240 pf	22372-241	1
	C9	· · Capacitor, Mica, 150 pf	22372-151	1
	C10	· · Capacitor, Mica, 82 pf	22372-820	1
	C11	· · Capacitor, Mica, 330 pf	22372-331	1
	C12	· · Capacitor, Mica, 750 pf	22373-751	1
	C13-C19, C21-C31, C33-C34, C36, C38, C39, C40, C45, C49, C50, C54, C56, C57, C60-C67, C72, C75, C76-C79, C81, C82, C94, C100, C101,C103, C104,C111, C112,C120, C121,C123,	· · Capacitor, Ceramic, 0.1 µf, 20%, 50 V	21732	56
	C20, C32 C52, C58, C80, C93, C102, C113	· · Capacitor, Tantalum, 15 µf, 20%, 20 V	25062-156	8
	C37	· · Capacitor, Ceramic, 1000 pf, 20% (ERIE 8101-050-651-102M)	21756	1

Table 6-6. Main IF/AF Converter Circuit Card Assembly (A4)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	C41	· · Capacitor, Ceramic, .022 µf, 20%	21762	1
	C42, C59, C83, C85, C91, C95, C96, C97, C98, C106	· · Capacitor, Tantalum, 6.8 µf, 20%, 35 V, (T362)	25060-685	10
	C55	· · Not Used		
	C43, C51, C53, C69, C70	· · Capacitor, Ceramic, 0.01 µf, 20% Erie 8121-050-651-103M	21733	5
	C44, C47	· · Capacitor, Mica, 1500 pf, 2%,	22114	2
	C46	· · Capacitor, Mica, 82 pf, 2%	22108	1
	C68	· · Capacitor, Mica, 3300 pf, 2%	22145	1
	C71	· · Capacitor, Mica, 100 pf, 2%, CM05F101G03	22109	1
	C73, C35	· · Capacitor, Electrolytic, 100 µf, 25 V, ET101X024A5	24066	2
	C74, C122	· · Capacitor, Ceramic, 1 µf, 20%, Erie 8131-050-651-105M	21748	2
	C84	· · Capacitor, Ceramic, 10 pf, 831-000-CONO-100C	21347	1
	C87, C114, C116	· · Capacitor, Tantalum, 1.0 µf, 35 V, T362	25060-105	3
	C88	· · Capacitor, Ceramic, 1500 pf, 10% Redcap	21735	1
	C89	· · Capacitor, Ceramic, 820 pf, 5%	22156	1
	C92	· · Capacitor, Electrolytic, 470 µf, 25 V, ET471X025A01	24058	1
	C99, C105, C108	· · Capacitor, Electrolytic, 220 µf, 16 V	24067	3
	C107,C118, C119	· · Capacitor, Tantalum, 68 µf, 20%, 15 V, T362	25063-686	3
	C115, C117	· · Capacitor, Ceramic, 390 pf	21765	2
	C86	· · Capacitor, Ceramic, 0.33 µf	25060-334	1

Table 6-6. Main IF/AF Converter Circuit Card Assembly (A4)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	CR1-CR16, CR18-CR31	· · Diode, 1N916	35514	30
	CR17	· · Not Used		
	FL1	· · LSB Filter, 3.0 kHz	07883-6	1
	FL2	· · USB Filter, 3.0 kHz	07883-5	1
	FL3	· · Bandpass Filter, 1.0 kHz	07883-1	1
	FL4	· · Bandpass Filter, 3.0 kHz	07883-2	1
	FL5	· · Bandpass Filter, 3.0 kHz	07883-3	1
	FL6	· · Bandpass Filter, 6.0 kHz	07883-4	1
	J1, J3, J4-J6	· · Connector, RF	60044	5
	J2	· · Connector, Ribbon, 40-Way, 3432-2003	61271	1
	J7	· · Connector, Ribbon, 26-Way, 3429-2003	61269	1
	J8	· · Connector, Ribbon, 34-Way, 3431-2003	61270	1
	L1, L2	· · Coil Assembly	08485	2
	L3	· · Coil Assembly	08531	1
	L4, L5	· · Choke, 100 µH, MS90538-12	43033	2
	L6	· · Choke, 10 µH	43029	1
	Q1, Q2, Q6-Q10	· · Transistor, 2N5089	32021	7
	Q3, Q4, Q5, Q11	· · Not Used		
	R1-R7 R9-R15, R23, R28, R55, R62, R66, R68, R70, R72, R77, R78	· · Resistor, Film, 4.7 K, 2%, 1/4 W	12161-472	29

Table 6-6. Main IF/AF Converter Circuit Card Assembly (A4)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R85, R87, R102,R144, R145			
	R153	• • Not Used		
	R8, R29, R46, R80, R82, R115	• • Resistor, Film, 47 ohms, 2%, 1/4 W	12161-470	6
	R79	• • Resistor, Film, 1 K, 2%, 1/4W		1
	R16-R22, R24, R33, R36, R40, R53, R57, R58, R71, R86, R88, R89, R130, R132, R135	• • Resistor, Film, 10 K, 2%, 1/4 W	12161-103	21
	R25, R60	• • Resistor, Film, 100 ohms, 2%, 1/4 W	12161-101	2
	R50, R92, R126, R136, R137	• • Resistor, Film, 4.7 K, 2%, 1/4 W	12161-472	5
	R26, R30, R49, R73, R83, R91, R124, R147, R61	• • Resistor, Film, 22 K, 2%, 1/4 W	12161-223	9
	R59, R148	• • Not Used		
	R27, R44, R64, R94, R113, R143	• • Resistor, Film, 1.5 K, 2%, 1/4 W	12161-152	6
	R31, R84, R109,R111, R112,R114, R116,R121	• • Resistor, Film, 3.3 K, 2%, 1/4 W	12161-332	8

Table 6-6. Main IF/AF Converter Circuit Card Assembly (A4)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R32, R38, R41, R52, R90, R93, R103	· · Resistor, Film, 47 K, 2%, 1/4 W	12161-473	7
	R34, R51, R101, R128	· · Resistor, Film, 2.2 K, 2%, 1/4 W	12161-222	4
	R35, R75, R110	· · Resistor, Film, 470 ohms, 2%, 1/4 W	12161-471	3
	R37, R95, R96, R117, R122,R123, R125,R139, R140, R150, R151	· · Resistor, Film, 100 K, 2%, 1/4 W	12161-104	11
	R39	· · Resistor, Trimmer, 2 K, 8014EMF202E1	16090-202	1
	R43, R48	· · Resistor, Film, 680 ohms, 2%, 1/4 W	12161-681	2
	R45	· · Resistor, Film, 330 K, 2%, 1/4 W	12161-334	1
	R47	· · Resistor, Trimmer, 50 K, 8014EMF503E1	16090-503	1
	R65, R69, R97, R107, R129,R131, R134	· · Resistor, Film, 15 K, 2%, 1/4 W	12161-153	7
	R67, R104	· · Resistor, Film, 18 K, 2%, 1/4 W	12161-183	2
	R42, R54, R63, R138 R149, R56, R141	· · Not Used		
	R98, R76	· · Resistor, Film, 12 K, 2%, 1/4 W	12161-123	2
	R99, R146	· · Resistor, Film, 27 K, 2%, 1/4 W	12161-273	2
	R100, R133	· · Resistor, Film, 10 ohms, 2%, 1/4 W	12161-100	2

Table 6-6. Main IF/AF Converter Circuit Card Assembly (A4)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R105	• • Resistor, Trimmer, 10 K, 8014EMF103E1	16090-103	1
	R106	• • Resistor, Film, 180 K, 2%, 1/4 W	12161-184	1
	R108, R81, R74	• • Resistor, Film, 6.8 K, 2%, 1/4 W	12161-682	3
	R118	• • Resistor, Film, 39 K, 2%, 1/4 W	12161-393	1
	R119	• • Resistor, Trimmer, 5 K, 8014EMF502E1	16090-502	1
	R120	• • Resistor, Film, 68 K, 2%, 1/4 W	12161-683	1
	R127	• • Resistor, Film, 8.2 K, 2%, 1/4 W	12161-822	1
	R142	• • Resistor, Film, 140 ohms, 2%, 1/4 W	12138	1
	R152	• • Resistor, Film, 1 M, 2%, 1/4 W	12161-105	1
	T1	• • Transformer Assembly	08535	1
	U1	• • Integrated Circuit, 4028	36575	1
	U2, U4, U13, U15, U23	• • Integrated Circuit, 4042	36613	5
	U3, U5, U16	• • Integrated Circuit, 40109	36790	3
	U6	• • Integrated Circuit, uA78L12AWC, T092	36760	1
	U7, U14, U17	• • Integrated Circuit, 324, LM324N	36784	3
	U8	• • Integrated, Circuit, A757, u6A7757393, Fairchild	36541	1
	U9	• • Integrated Circuit, 4013	36588	1
	U10	• • Integrated Circuit, CA3046	36785	1
	U11, U12	• • Integrated Circuit, 4066	36792	2
	U18	• • Integrated Circuit, MC1357	36631	1
	U19	• • Integrated Circuit, 4053B (Alternate 40097)	36801	1
	U20	• • Integrated Circuit, MC1496P	36748	1
	U21	• • Integrated Circuit, AD7524	36803	1
	U22, U28	• • Integrated Circuit, 1458	36673	2
	U24	• • Integrated Circuit, 339, LM339	36693	1
	U25	• • Integrated Circuit, CD22100	36802	1

Table 6-6. Main IF/AF Converter Circuit Card Assembly (A4)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	U26	• • Integrated Circuit, LM1877-9	36777	1
	U27	• • Integrated Circuit, uA7815UC	36708	1
	U29	• • Not Used		
	U30, U31	• • Integrated Circuit, MC3340	36763	2
		• • Screw, #4-40 x 5/16" Lg.*	76013	3
		• • Washer, Flat #4*	75022	3
		• • Washer, Split Lock #4*	75002	3
		• • Nut, Hex #4*	75203	3
		• • Wire, Bus Wire #24*	58007	1
		• • Sleeving, PTFE Tubing #24*	59528	1
		• • Socket for .040 Dia. Pin*	61177	17
		• • Socket for .100 Dia. Pin*	61178	14
		• • Beads, Ceramic*	70854	2
		• • Terminal*	70099	17
		• • Plug, Shorting, Red, Cambion 461-2871-01-03-12*	61348-2	1

*NOTE: These components are not shown on illustration.

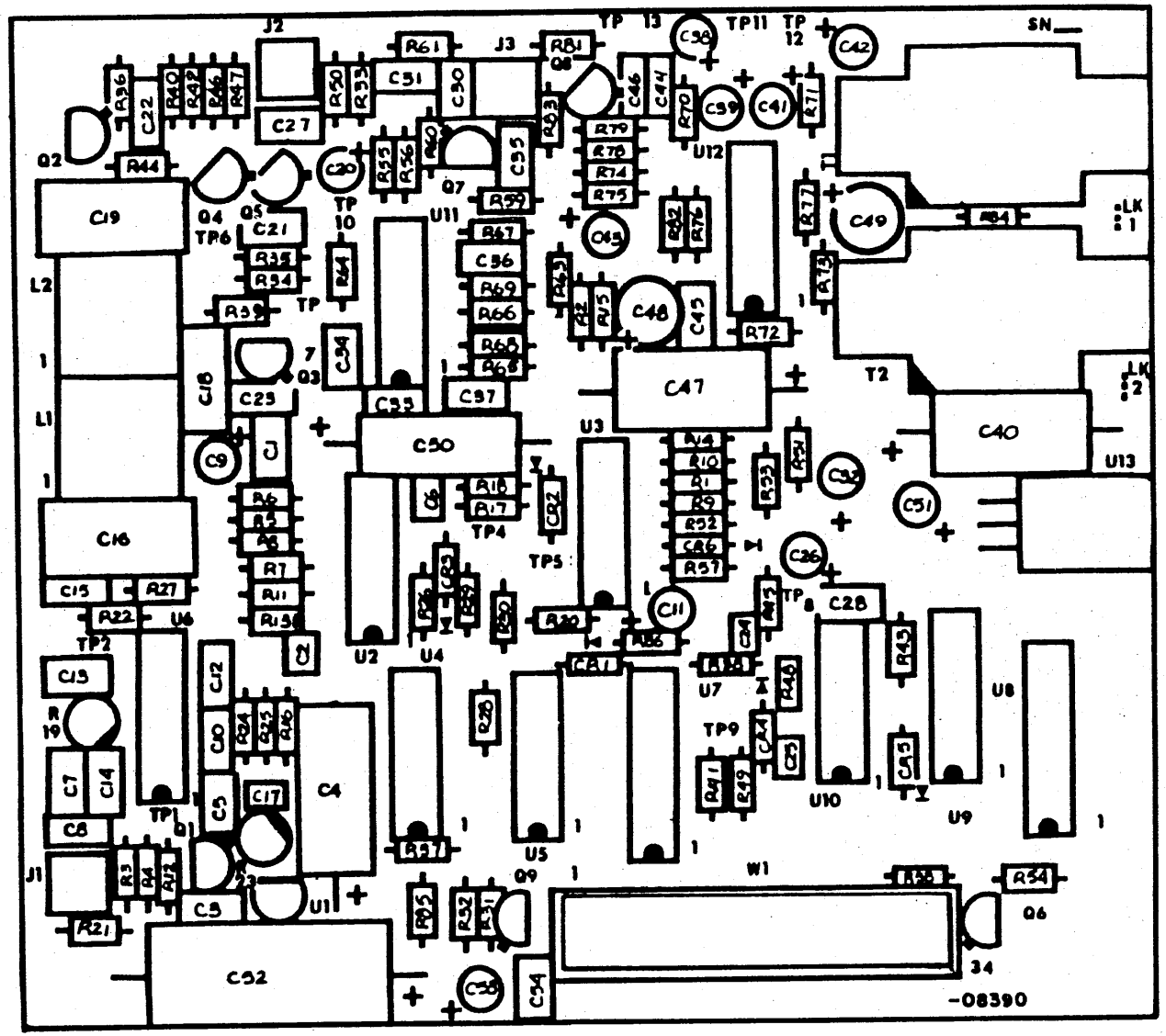


Figure 6-10. ISB Circuit Card Assembly (A5) Component Location Diagram

Table 6-7. ISB Circuit Card Assembly (A5) Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A5	ISB Circuit Card Assembly	08390	1
	C1, C3, C5, C7, C8, C10, C12-C15, C20, C21, C23, C27, C28, C30, C31, C33, C34-C37, C45, C54	· Capacitor, Ceramic, 0.1 µf, 50 V, ±20%	21732	24
	C2	· Capacitor, Ceramic, 1000 pf, 18 V, ±20%	21756	1
	C4, C50	· Capacitor, Electrolytic, 100 µf, 25 V, -10 +50%	24066	2
	C6	· Capacitor, Ceramic, 0.022 µf, 50 V, ±20%	21762	1
	C9, C20, C26, C53	· Capacitor, Tantalum, 15 µf, 20 V, ±20%	25062-156	4
	C11, C32, C38, C39, C41, C42, C43, C51	· Capacitor, Tantalum, 6.8 µf, 35 V, ±20%	25060-685	8
	C16, C19	· Capacitor, Mica, 1500 pf, 500 V, ±2%	22174	2
	C17, C24, C25	· Capacitor, Ceramic, 0.01 µf, 50 V, ±20%	21733	3
	C18	· Capacitor, Mica, 82 pf, 500 V, ±2%	22108	1
	C29	· Not Used		
	C40, C47	· Capacitor, Electrolytic, 220 µf, 16 V, -10 +50%	24067	2

Table 6-7. ISB Circuit Card Assembly (A5)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	C44	· Capacitor, Ceramic, 4700 pf, 50 V, ±5%	21778	1
	C46	· Capacitor, Ceramic, 2200 pf, 50 V, ±5%	21779	1
	C48, C49	· Capacitor, Tantalum, 68 µf, 15 V, ±20%	25063-686	2
	C52	· Capacitor, Electrolytic, 470 µf, 25 V -10 +100%	24058	1
	CR1-CR6	· Diode, Silicon, 1N916	35514	6
	J1-J3	· Connector, RF	60044	3
	L1, L2	· Coil, RF, Variable	08485	2
	Q1-Q9	· Transistor, NPN, High Power	32021	9
	R1, R5, R26, R32, R37, R41, R54, R58	· Resistor, Film, 22 K, ±2%, 1/4 W	12161-223	8
	R2, R18, R38	· Resistor, Film, 1.5 K, ±2%, 1/4 W	12161-152	3
	R3	· Resistor, Film, 56 K, ±2%, 1/4 W	12161-563	1
	R4, R52	· Resistor, Film, 12 K, ±2%, 1/4 W	12161-123	2
	R6, R65, R66, R67, R69	· Resistor, Film, 3.3 K, ±2%, 1/4 W	12161-332	5
	R7, R25, R81	· Resistor, Film, 2.2 K, ±2%, 1/4 W	12161-222	3
	R8, R64, R47	· Resistor, Film, 470 ohms, 2%, 1/4 W	12161-471	3

Table 6-7. ISB Circuit Card Assembly (A5)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R9, R13, R15, R28	· Resistor, Film, 47 K, ±2%, 1/4 W	12161-473	4
	R10, R11, R14, R29, R34, R35, R43, R56, R63	· Resistor, Film, 10 K, ±2%, 1/4 W	12161-103	9
	R12, R30, R36, R39, R42, R44, R48, R51, R53, R59	· Resistor, Film, 1 K, ±2%, 1/4 W	12161-102	10
	R16, R22, R33, R50	· Resistor, Film, 47 ohms, ±2%, 1/4 W	12161-470	4
	R17, R24	· Resistor, Film, 680 ohms, ±2%, 1/4 W	12161-681	2
	R19	· Resistor, Trimmer, 2 K	16090-202	1
	R20	· Resistor, Film, 330 K, ±2%, 1/4 W	12161-334	1
	R21	· Resistor, Film, 100 ohms, ±2%, 1/4 W	12161-101	1
	R23	· Resistor, Trimmer, 50 K	16090-503	1
	R27, R72, R73, R78	· Resistor, Film, 4.7 K, ±2%, 1/4 W	12161-472	4
	R31, R40, R62, R80	· Not Used		
	R45, R70, R71	· Resistor, Film, 15 K, ±2%, 1/4 W	12161-153	3
	R49	· Resistor, Film, 18 K, ±2%, 1/4 W	12161-183	1
	R55	· Resistor, Film, 33 K, ±2%, 1/4 W	12161-333	1
	R46, R57	· Resistor, Film, 6.8 K, ±2%, 1/4 W	12161-682	2

Table 6-7. ISB Circuit Card Assembly (A5) Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R60	· Resistor, Film, 33 ohms, ±2%, 1/4 W	12161-330	1
	R61	· Resistor, Film, 390 ohms, ±2%, 1/4 W	12161-391	1
	R68	· Resistor, Film, 1.2 K, ±2%, 1/4 W	12161-122	1
	R74	· Resistor, Film, 39 K, ±2%, 1/4 W	12161-393	1
	R75	· Resistor, Film, 68 K, ±2%, 1/4 W	12161-683	1
	R76, R77	· Resistor, Film, 100 K, ±2%, 1/4 W	12161-104	2
	R79	· Resistor, Film, 8.2 K, ±2%, 1/4 W	12161-822	1
	R82, R84	· Resistor, Film, 140 ohms, ±2%, 1/4 W	12138	2
	R83	· Resistor, Film, 22 ohms, ±22%, 1/4 W	12161-220	1
	R85	· Resistor, Film, 10 ohms, ±2%, 1/4 W	12161-100	1
	R86	· Resistor, Film, 1 Meg., ±2%, 1/4 W	12161-105	1
	T1, T2	· Transformer Assembly, Audio	08535	2
	U1	· Integrated Circuit, +12 Volt Regulator	36760	1
	U2	· Integrated Circuit, Transistor Array	36785	1
	U3, U10	· Integrated Circuit, Quad Operational Amplifier	36784	2
	U4	· Integrated Circuit, Dual D Flip-Flop	36588	1
	U5, U9	· Integrated Circuit, Quad Bilateral Switch	36792	2
	U6	· Integrated Circuit, Operational Amp.	36541	1
	U7, U8	· Integrated Circuit, Quad Latch	36613	2
	U11	· Integrated Circuit, Product Detector	36748	1
	U12	· Integrated Circuit, Dual Audio Amplifier, 2 Watt	36777	1
	U13	· Integrated Circuit, +15 Volt Regulator	36708	1
	W1	· Cable, Ribbon	08486	1
	W10	· Cable Assembly	08555-6	1
	W11	· Cable Assembly, Coaxial	08555-7	1

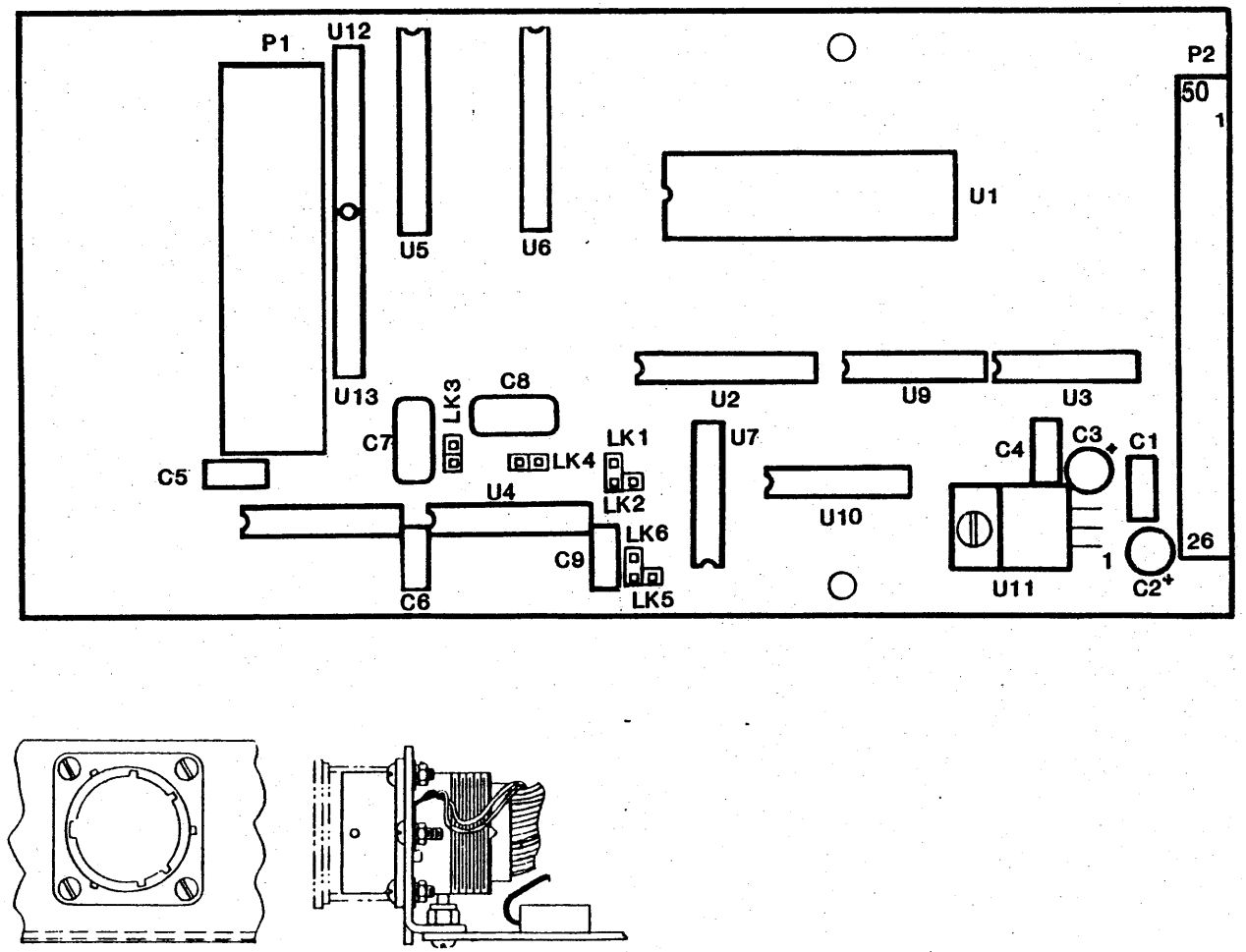


Figure 6-11. Asynchronous Interface Assembly (A6A1)
(RS-232C Remote Control Interface Circuit Card)
Component Location Diagram

Table 6-8. Serial Asynchronous Interface Assembly (A6A1)
RS-232C Remote Control Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A6A1	RS-232C Remote Control Interface Circuit Card Assembly (Schematic Diagram 09972)	A09970-1	1
		· Printed Circuit Card Wiring Assembly	D09971	1
	C1, C4	· · Capacitor, Fixed, Ceramic, 0.1 µf, ±20%, 50 V	21732	2
	C2, C3	· Capacitor, Fixed, Tantalum, 6.8 µf, ±20%, 35 V	25060-685	2
	C5, C6, C9	· · Capacitor, Fixed, Ceramic, .01 µf, ±20%, 35 V	21733	3
	C7, C8	· · Capacitor, Fixed, Mica, 300 pf, ±5%, 500 V	22035	2
	P2	· · Connector, 50 pin, 2 Section	A08491	1
	U1,	· · Integrated Circuit, 8251A, UART	36952	1
	U2	· · Integrated Circuit, COM8116-5, Dual Baud Rate Generator	36953	1
	U3	· · Integrated Circuit, 26LS32 Quad Differential Line Receiver	36798	1
	U4	· · Integrated Circuit, 26LS30 Line Driver	36797	1
	U5, U6	· · Integrated Circuit, 74LS244 Octal Bus Driver	36753	2
	U7	· · Oscillator, Clock, 4.9152 MHz	37050	1
	U8	· · Integrated Circuit, 74LS32 Quad 2-Input OR GATE	36640	1
	U9	· · Integrated Circuit, 74LS00 Quad 2-input NAND Gate	36632	1
	U10	· · Integrated Circuit, 74LS74 Dual D Flip Flop	36636	1
	U11	· · Integrated Circuit, 7905 Voltage Regulator	36704	1
	U12, U13	· · Resistor, Network, 2.2 K, 7 Resistors, 8 Pin SIP	19321-222	2

Table 6-8. Serial Asynchronous Interface Assembly (A6A1)
RS-232C Remote Control Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	W1	· · Cable Assembly	C08493	1
	W1J1	· · Connector, 26 Pin, (p/o W1) (M8372302R1626N)	61091	1
		· · Connector, 26 Pin, (mate W1J1) M8723-13R 1626N*	61092	1
		· · Connector, Receptacle, PCB*	61371-01	2
		· · Connector, Receptacle, PCB*	61371-02	4
		· · Connector, Shorting Socket 2 pos, .100 CTRS*	70124	4
		· · Backshell, Connector MS3417-16N*	61093	1
		· · Plate, Connector, Mtg.*	C08471	1
		· · Screw, Pan Head, #4-40 (Ref. W1J1 and U11)*	75002	6
		· · Washer, Split Lock, #4-40 (Ref. W1J1)*	75002	6
		· · Nut, Hex #4-40 (Ref. W1J1)*	75203	6
		· · Hex, Elastic Stop-Nut #4-40*	75462	2
		· · Screw, Pan Head, #4-40 x 3/8 Lg.*	76014	2

*NOTE: These components are not shown on illustration.

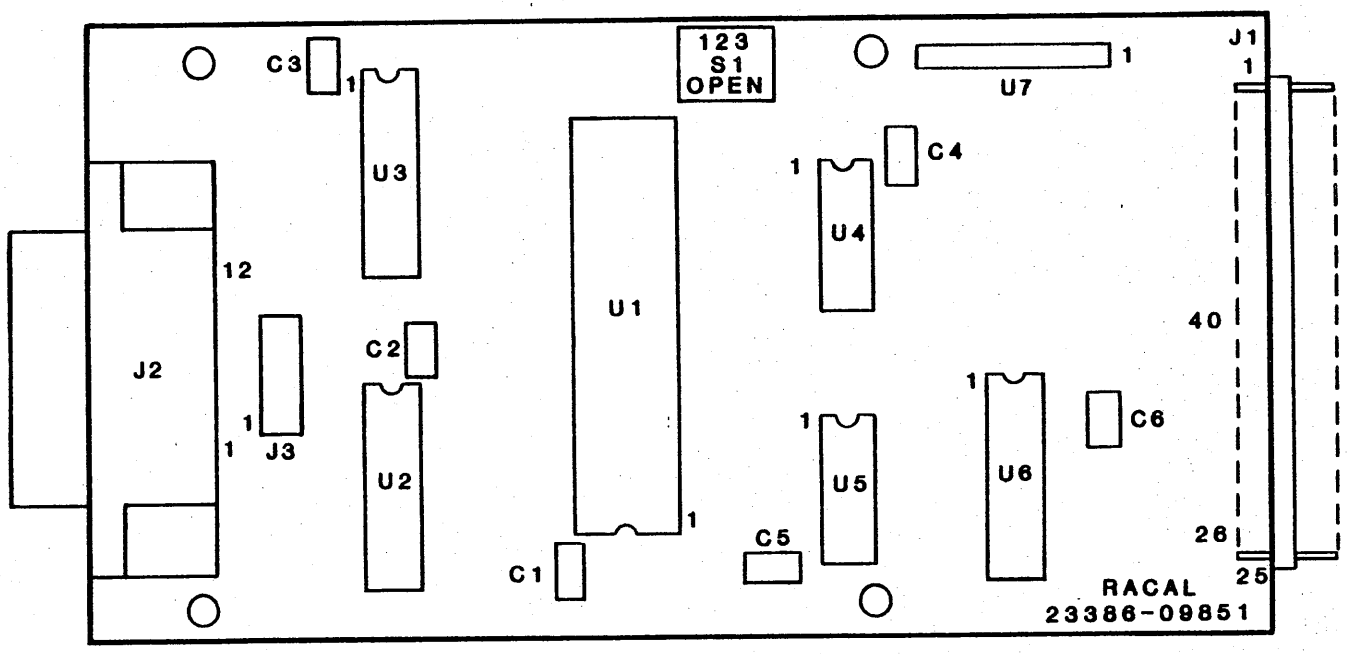


Figure 6-11A. Z80 GPI Interface Circuit Card Assembly (A6A1)
(IEEE-488C Circuit Card Assembly)
Component Location Diagram

Table 6-8A. Z80 GPI Interface Circuit Card Assembly (A6A1) (IEEE-488C Interface Circuit Card Assembly) Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A6A1	Z80 GPI Interface Circuit Card Assembly (Schematic Diagram 07974)	A09851	1
		• Printed Circuit Card Wiring Assembly	D07975	1
	A1	• • Sub-assembly, Address Switch, Circuit Card	B07895	1
	A1W1	• • • Cable Assembly, Ansley FSN23B-6 (Ref. A1)	55232	1
		• • • Plate, Connector Switch (Ref. A1)	B07983	1
	S1	• • • Switch, DIP, CTS 206-3	52527	1
	C1-C6	• • Capacitor, Tantalum, .01 µf	21733	6
	J1	• • Connector, Berg, 50-Pin, 2 Section	A07881	1
	J2	• • Connector, Amp Champ, #552791-1	61257	1
	J3	• • Socket Assembly, Ansley 741	61253	6
	R1	• • Resistor, Film, 1 K, ±2%	12161-102	1
	S1	• • Switch, CTS 206-3	52427	1
	U1	• • Integrated Circuit, TMS 9914	36881	1
	U2	• • Integrated Circuit, 75160, Interface Bus Transceiver	36882	1
	U3	• • Integrated Circuit, 75161, Interface Bus, Transceiver	36883	1
	U4	• • Integrated Circuit, 74LS04, Hex Inverter	36676	1
	U5	• • Integrated Circuit, 74LS08,	36734	1
		Quadruple 2-Input Positive-And-Gate	36734	1
	U6	• • Integrated Circuit, 74LS244, Octal Buffer	36753	1
	U7	• • Integrated Circuit, 10 Pin SIP	19323-103	1

Table 6-8A. Z80 GPI Interface Circuit Card Assembly (A6A1)
(IEEE-488C Interface Circuit Card Assembly)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
		· · Plate, Connector-Switch, Mounting Plate (A6A1A1)	B07983	1
		· · Screw, Pan Head, #4-40 x 5/16 Lg.*	76013	4
		· · Washer, Split Lock, #4*	75002	4
		· · Washer, Flat, #4*	75022	4
		· · Hardware Kit, Connector-to-A6A1A1 Mounting Screws (AMP #552633-4)	61256	1
		· · ROMSET to replace 1600002 on the A6A2 Microprocessor Assembly (A09817) A6A2, U5, U6, U14	1600003	1

*NOTE: These components are not shown on illustration; quantity of two used in A07976-1 configuration.

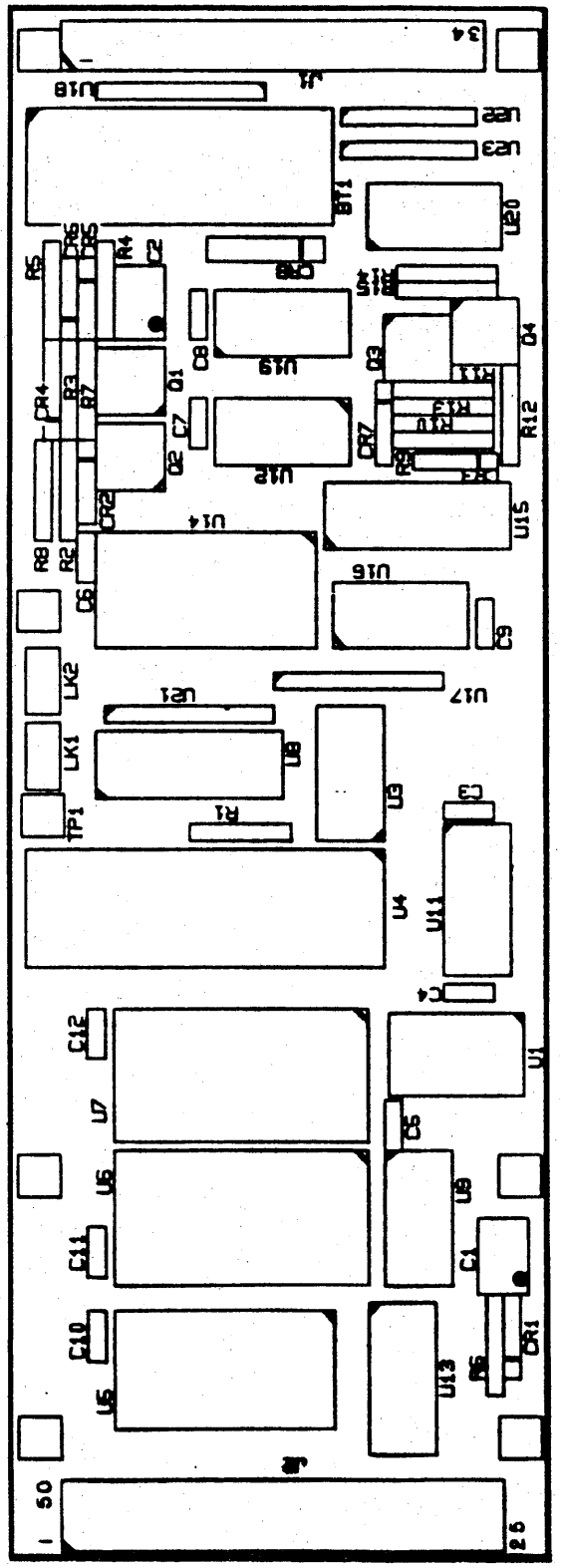


Figure 6-12. Microprocessor Circuit Card Assembly (A6A2)
Component Location Diagram

Table 6-9. Microprocessor Circuit Card Assembly (A6A2) Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A6A2	Microprocessor Circuit Card Assembly (Schematic No. 4200018)	4100030	1
		· Printed Circuit Card Wiring Assembly	4300012	1
	BT1	· · Battery, Memory Retain, GE DS2SD, 2.4 V	42517	1
	C1	· · Capacitor, Tantalum, 6.8 µf	25061-685	1
	C2	· · Capacitor, Tantalum, 4.7 µf	25060-475	1
	C3-C6, C8, C9, C11, C12	· · Capacitor, Ceramic, 0.1 µf	21732	8
	C7, C10	· · Capacitor, Ceramic, 1 µf	21748	2
	CR1-CR3, CR5, CR6	· · Diode, 1N916	35514	1
	CR4	· · Diode, 1N270	35538	1
	CR7	· · Diode, 1N752A	33543	1
	CR8	· · Diode, Suppressor, MPTE-5	36009	1
	J1	· · Connector, 34 Pin, Header	61200	1
	J2	· · Connector, 50 Pin, Socket	61225	1
	Q1, Q2, Q4	· · Transistor, 2N3904	32036	3
	Q3	· · Transistor, 2N3906	32037	1
	R1	· · Resistor, Film, 330 K, 2%	12161-331	1
	R2, R9, R15	· · Resistor, Film, 47, 2%	12161-470	1
	R3	· · Resistor, Film, 47, 2%	12161-470	1
	R4, R8, R13	· · Resistor, Film, 10 K, 2%	12161-103	3
	R5	· · Resistor, Film, 270, 2%	12161-271	1
	R6	· · Resistor, Film, 100 K, 2%	12161-104	1
	R7	· · Resistor, Film, 5.6 K, 2%	12161-562	1
	R10	· · Resistor, Film, 82 K, 2%	12161-823	1
	R11	· · Resistor, Film, 39 K, 2%	12161-393	1
	R12	· · Resistor, Film, 120 K, 2%	12161-124	1
	R14	· · Resistor, Film, 47 K, 2%	12161-473	1
	U1	· · Oscillator, 4 MHz Clock, XO-12B, Dale	37046	1

Table 6-9. Microprocessor Circuit Card Assembly (A6A2) Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	U2	· · Not Used		
	U3	· · Integrated Circuit, 74LS04	36676	1
	U4	· · Integrated Circuit, Z80, CPU	36887	1
	U5	· · Integrated Circuit, HM6116LP-3, RAM	36824	1
	U7	· · Integrated Circuit, ROM	1600016	1
	U8	· · Integrated Circuit, 74LS641	36885-0641	1
	U9	· · Integrated Circuit, 74LS74	36636	1
	U10	· · Not Used		
	U11, U13	· · Integrated Circuit, 74LS138	36714	2
	U12	· · Integrated Circuit, 74LS32	36640	1
	U14	· · Integrated Circuit, 8253	36888	1
	U15	· · Integrated Circuit, 74LS244	36753	1
	U16	· · Integrated Circuit, 74LS30	36635	1
	U17, U21	· · Integrated Circuit, 10 K, Resistor, Network, 9 Res., 10 Pin SIP	19323-103	2
	U18	· · Integrated Circuit, 4.7 K, Resistor, Network, 9 Res., 10 Pin SIP	19323-472	1
	U19, U20	· · Integrated Circuit, 7407	36565	2
	U22, U23	· · Integrated Circuit, 2.2 K, Resistor, Network, 7 Res., 8 Pin SIP	19321-222	2
		· · Wire, Buss #22 (for links 1-2)*	58006	1
		· · Sleeving, PFTE Tubing #22* (for use with 46)	59537	1
		· · Socket, IC, 28-Pin, DIP*	70636-28	2
		· · Socket, IC, 40-Pin, DIP*	61313	1

*NOTE: These components are not shown on illustration.

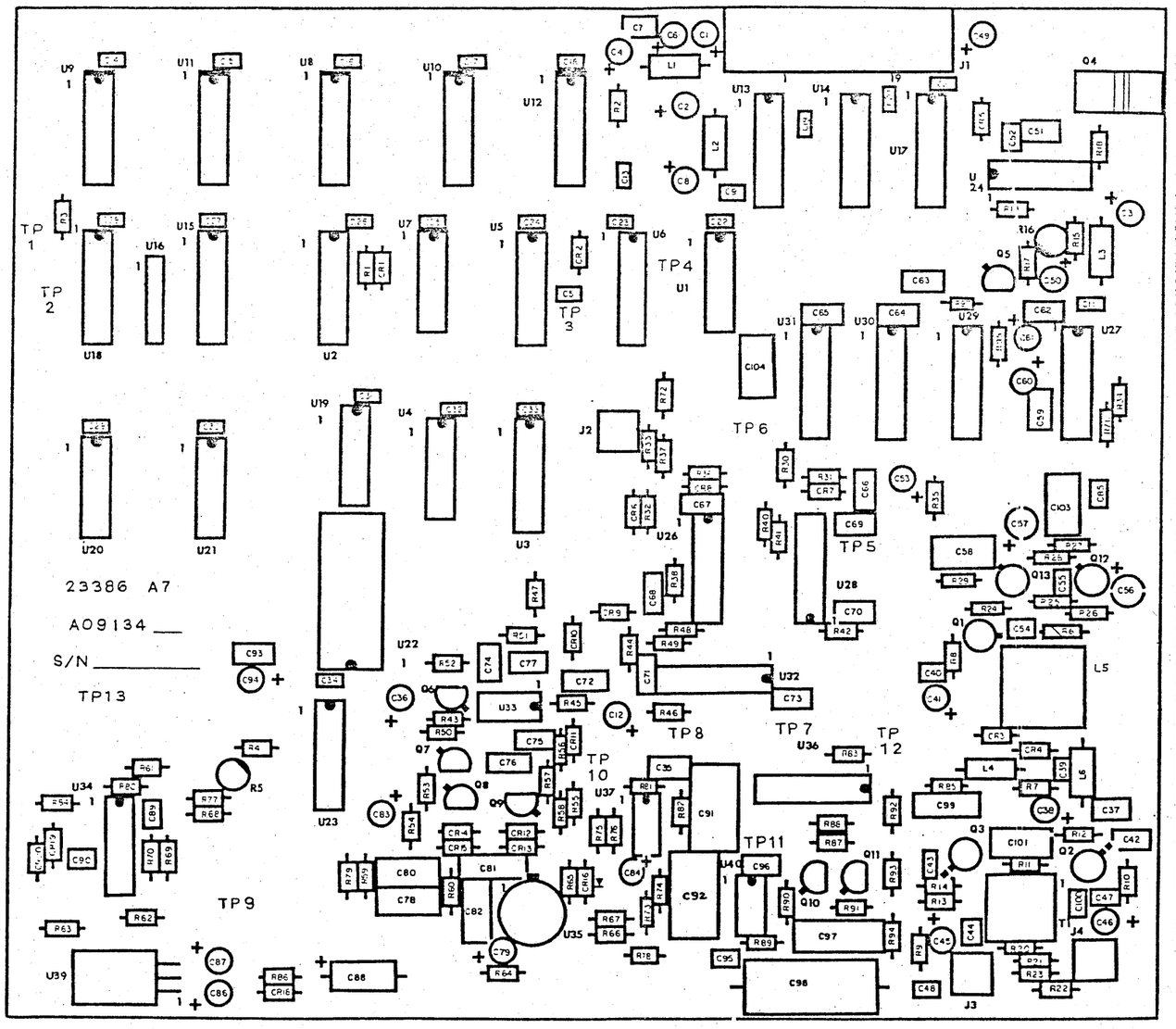


Figure 6-13. 1st LO Synthesizer Circuit Card Assembly (A7) Component Location Diagram (09134)

Table 6-10. 1st LO Synthesizer Circuit Card Assembly (A7) Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A7	1st LO Synthesizer Circuit Card Assembly (Schematic No. 09256)	A09134	1
		· Printed Circuit Card Wiring Assembly	E09135	1
	C1-C4, C6, C8, C12, C36, C38, C45, C46, C49, C50, C57, C60, C61, C79, C83, C84, C94	· · Capacitor, Tantalum, 6.8 µf, 35 V, ±20%	25060-685	20
	C5, C7, C9, C11, C13-C34, C39, C44, C47, C48, C55, C85	· · Capacitor, Ceramic 0.01 µf, ±20%, 100 V	21733	32
	C35, C37, C42, C51, C59, C62, C63-C77, C93, C96	· · Capacitor, Ceramic, 0.1 µf, ±20% 100 V	21732	23
	C40, C43 C52, C54 C95	· · Capacitor, Ceramic, 0.001 µf, ±20%, 100 V	21756	5
	C41, C56	· · Capacitor, Tantalum, 33 µf, ±10%, 25 V	25061-336	2
	C53	· · Capacitor, Tantalum, 150 µf, ±20%, 6 V	25065-157	1
	C58	· · Capacitor, Mica., 10 pf, ±1/2 pf, 500 V, CM05	22001	1
	C78	· · Capacitor, Mica., 100 pf, ±5%, 100 V, CM05	22023	1
	C80	· · Capacitor, Mica., 27 pf, ±2%, 100 V, CM05	22119	1

Table 6-10. 1st LO Synthesizer Circuit Card Assembly (A7)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	C81	· · Capacitor, Polyester, 0.001 µf, ±10%, 400 V	26899	1
	C82	· · Capacitor, Polycarbonate, 0.047 µf, ±10%, 100 V	26896	1
	C86, C87	· · Capacitor, Tantalum, 1 µf, ±10%, 35 V	25060-105	2
	C88	· · Capacitor, Tantalum, 15 µf, ±20%, 20 V, CS13	25035	1
	C89	· · Capacitor, Ceramic, 0.047 µf, ±20%, 100 V	21759	1
	C90	· · Capacitor, Ceramic, 2200 pf, ±20%, 100 V	21780	1
	C91	· · Capacitor, Mica., 4700 pf, ±5% 100 V, CM05	22066	1
	C92	· · Capacitor, Mica., 2200 pf, ±5%, 100 V, CM05	22057	1
	C97	· · Capacitor, Polycarbonate, 1.0 µf, ±10%, 100 V	26875	1
	C98	· · Capacitor, Polycarbonate, 3.3 µf, ±10%, 63 V	26897	1
	C99	· · Capacitor, Polycarbonate, 0.068 µf, ±10%, 100 V	26898	1
	C100	· · Capacitor, Ceramic 4.7 pf, 8101, Erie	21783	1
	C101	· · Capacitor, Mica., 82 pf, ±2%, 500 V, CM05	22108	1
	C10, C102	· · Not Used		
	C103, C104	· · Capacitor, Mica., 47 pf, ±5%, 500 V, CM05	22014	2

Table 6-10. 1st LO Synthesizer Circuit Card Assembly (A7) Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	CR1, CR2, CR5-CR16, CR19, CR20	· · Diode, Silicon, 1N916	35514	16
	CR3, CR4	· · Diode, Varactor, KV2201	29016	2
	CR17, CR2	· · Not Used		
	CR18	· · Diode, Zener, 1N757A, 9.1 V	33544	1
	J1	· · Connector, PCB, Rt. Angle, 20-Way, 3M#3492-1002	61276	1
	J2-J4	· · Connector, PCB, Coax, SMB, Male	60044	3
	L1-L4	· · Choke, Fixed, RF, 6.8 µH	43028	4
	L5	· · Coil Assembly, Variable	09255	1
	L6	· · Choke, Fixed, RF, 15 µH	43030	1
	Q1	· · Transistor, FET, 2N4416	32508	1
	Q2, Q3	· · Transistor, NPN, Power, RF, MR517	32044	2
	Q4	· · Transistor, NPN, Power, 2N4921	32039	1
	Q5, Q13	· · Transistor, NPN, 2N2369	32255	2
	Q6, Q7, Q8, Q11	· · Transistor, PNP, Plastic, 2N4126	31508	4
	Q12	· · Transistor, NPN, 2N918	31500	1
	R1, R87, R89	· · Resistor, Film, 47 K, 2%, 1/4 W	12161-473	3
	R2, R12, R28, R72, R92, R94	· · Resistor, Film, 10 ohm, 2%, 1/4 W	12161-100	6
	R3, R50, R62, R73, R81-R83	· · Resistor, Film, 10 K, 2%, 1/4 W	12161-103	7
	R4, R91	· · Resistor, Film, 150 ohm, 2%, 1/4 W	12161-151	2
	R5	· · Resistor, Variable, 200 ohm	16090-201	1
	R6, R29, R85	· · Resistor, Film, 100 ohm, 2%, 1/4 W	12161-101	3
	R7, R8, R14, R23	· · Resistor, Film, 68 ohm, 2%, 1/4 W	12161-680	4

Table 6-10. 1st LO Synthesizer Circuit Card Assembly (A7)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R9, R22, R60	· · Resistor, Film, 22 ohm, 2%, 1/4 W	12161-220	3
	R10, R26	· · Resistor, Film, 1.5 K, 2%, 1/4 W	12161-152	2
	R11, R93	· · Resistor, Film, 680 ohm, 2%, 1/4 W	12161-681	2
	R13	· · Resistor, Film, 390 ohm, 2%, 1/4 W	12161-391	1
	R15, R30, R33, R37, R47	· · Resistor, Film, 820 ohm, 2%, 1/4 W	12161-821	5
	R16	· · Resistor, Variable, 500 ohm	16090-501	1
	R17, R52, R56	· · Resistor, Film, 2.2 K, 2%, 1/4 W	12161-222	3
	R18	· · Resistor, Film, 47 ohm, 2%, 1/4 W	12161-470	1
	R19	· · Resistor, Comp. 1 ohm, 5%	12153	1
	R21, R27	· · Resistor, Film, 330 ohm, 2%, 1/4 W	12161-331	2
	R24, R34, R35, R38, R40-R44, R46, R48, R49, R55, R58, R86	· · Resistor, Film, 470 ohm, 2%, 1/4 W	12161-471	15
	R25, R61, R63, R68, R70, R90, R95, R97	· · Resistor, Film, 1 K, 2%, 1/4 W	12161-102	8
	R31, R32, R36	· · Resistor, Film, 220 ohm, 2%, 1/4 W	12161-221	3
	R39	· · Not Used		
	R45	· · Resistor, Film, 56 K, 2%, 1/4 W	12161-563	1
	R51	· · Resistor, Film, 4.7 K, 2%, 1/4 W	12161-472	1
	R53, R54, R59, R69, R84	· · Resistor, Film, 3.3 K, 2%, 1/4 W	12161-332	1

Table 6-10. 1st LO Synthesizer Circuit Card Assembly (A7)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R57	· · Resistor, Film, 3.9 K, 2%, 1/4 W	12161-392	1
	R64	· · Resistor, Film, 39 K, 2%, 1/4 W	12161-393	1
	R65, R74, R75, R76	· · Resistor, Film, 15 K, 2%, 1/4 W	12161-153	1
	R66	· · Resistor, Film, 8.2 K, 2%, 1/4 W	12161-822	1
	R67, R79	· · Resistor, Film, 12 K, 2%, 1/4 W	12161-123	2
	R71	· · Resistor, Film, 82 ohm, 2%, 1/4 W	12161-820	1
	R77	· · Resistor, Film, 100 K, 2%, 1/4 W	12161-104	1
	R78	· · Resistor, Film, 2.7 K, 2%, 1/4 W	12161-272	1
	R80	· · Resistor, Film, 150 K, 2%, 1/4 W	12161-154	1
	R88	· · Resistor, Film, 120 K, 2%, 1/4 W	12161-124	1
	R20	· · Resistor, Film, 39 ohm, 2%, 1/4 W	12161-390	1
	T1	· · Transformer, Wideband	08502-1	1
	U1	· · Integrated Circuit, 4001	36569	1
	U2	· · Integrated Circuit, 4503	36694	1
	U3, U5, U6	· · Integrated Circuit, 74LS174	36715	3
	U4	· · Integrated Circuit, 74LS02	36660	1
	U7	· · Integrated Circuit, 4070	36653	1
	U8-U14	· · Integrated Circuit, 4094	36767	7
	U15	· · Integrated Circuit, 82S83	36768	1
	U16	· · Integtated Circuit, Resistor Network, 6-Pin, 10 K	19324-103	1
	U17	· · Integrated Circuit, 4008	36570	1
	U18	· · Integrated Circuit, 40174	36766	1
	U19	· · Integrated Circuit, 74LS74	36636	1
	U20, U21	· · Integrated Circuit, 4006	36769	2
	U22	· · Integrated Circuit, 40108	36770	1
	U23	· · Integrated Circuit, DAC 20	36771	1
	U24	· · Integrated Circuit, µf A723	36728	1
	U25, U38	· · Not Used		
	U26, U28	· · Integrated Circuit, 10231	36774	2

Table 6-10. 1st LO Synthesizer Circuit Card Assembly (A7)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	U27	• • Integrated Circuit, 11C90	36745	1
	U29	• • Integrated Circuit, 74LS169	36772	1
	U30, U31	• • Integrated Circuit, 74LS168	36773	2
	U32	• • Integrated Circuit, 10211	36775	1
	U33, U37	• • Integrated Circuit, OP AMP, 1458	36776	2
	U34	• • Integrated Circuit, LM339	36693	1
	U35	• • Integrated Circuit, AD518	36765	1
	U36	• • Integrated Circuit, Analog Switch, DG201	36815	1
	U39	• • Integrated Circuit, 7812, Voltage Regulator	36707	1
	U40	• • Integrated Circuit, 3140E, FET, I/P Op Amp	36817	1
		• • Transistor Pad (Ref. Q1, Q5, Q12, Q13)*	70752	4
		• • Transistor Pad (Ref. Q2, Q3)*	70764	1
		• • Transistor Pad, 8-Pin*	70770	1
		• • Tubing, PTFE #24*	59538	1
		• • Wire, #24*	58007	1
		• • Screw, Pan Head #4-40 x 5/16 Lg.*	76013	1
		• • Washer, Flat #4*	75022	3
		• • Washer, Split Lock, #4*	75002	2
		• • Nut, Hex, #4*	75203	2
		• • Washer, Insulator-Round*	70793	1
		• • Compound, Thermal,* Wakefield #128*	91012	1
		• • Bracket, Transistor, Mtg.*	B08707	1
		• • Screw, Pan Head, #4-40 x 3/8" Lg.*	76014	1
		• • Beads, Ceramic*	70854	12

*NOTE: These components are not shown on illustration.

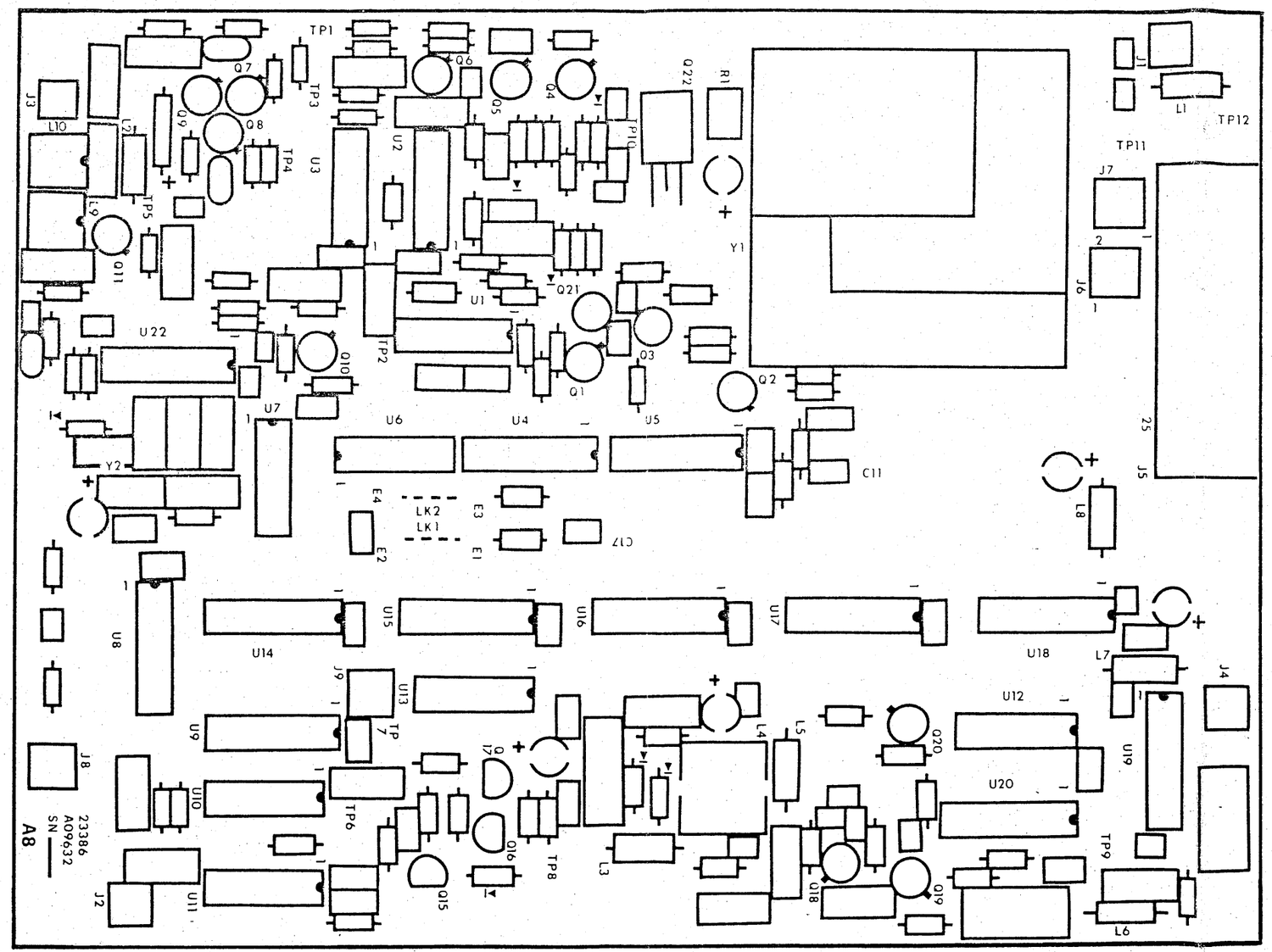


Figure 6-14. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8) Component Location Diagram

Table 6-11. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A8	2nd LO/BFO Synthesizer Circuit Card Assembly (Schematic No. 09633)	A09632	1
		· Printed Circuit Card Wiring Assembly	E09634	1
	C1, C23 C49, C54, C79, C81	· · Capacitor, Tantalum, 6.8 µf, ±20%, 35 V	25060-685	6
	C2, C34, C35, C37, C46, C56, C57	· · Capacitor, Mica, 100 pf, +5%, 500 V, CM05F101J03	22023	7
	C3, C4, C9, C11, C12, C13, C15-C19, C21, C22 C24, C27, C30, C39, C43-C45, C47, C48, C62, C66, C67-C71 C73, C74	· · Capacitor, Ceramic, 0.1 µf, ±20%, 50 V	21732	31
	C5, C8, C14, C32, C42, C52, C53, C58, C59-C61, C72, C78, C80	· · Capacitor, Ceramic, 0.01 µf, ±20%, 50 V	21733	14
	C6, C7	· · Capacitor, Ceramic, 0.047 µf, ±20%, 50 V	21759	2
	C36, C40, C87	· · Capacitor, Ceramic, 0.001 µf, +20%, 50 V	21756	3

Table 6-11. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	C20	· · Capacitor, Mica, 12 pf, ±5%, 500 V	22002	1
	C25	· · Capacitor, Tantalum, 3.3 µf, 10%, 15 V	25066	1
	C26, C51	· · Capacitor, Polycarbonate, 0.1 µf, 20%, 100 V	26871	2
	C28, C64	· · Capacitor, Mica, 150 pf, ±2%, 500 V, CM05F151G03	22101	2
	C29, C31, C83, C86	· · Capacitor, Mica, 39 pf, ±2%, 500 V, CM05E390G03	22100	4
	C33, C41	· · Capacitor, Mica, 68 pf, ±2%, 500 V, CM05F680G03	22100	4
	C38, C88	· · Capacitor, Mica, 5 pf ±1/2 pf, 500 V	22175	2
	C50	· · Capacitor, Polycarbonate, 0.47 µf, 20%, 100 V	26874	1
	C55	· · Capacitor, Mica, 56 pf, ±5%, 500 V, CM05E560J03	22017	1
	C63, C65	· · Capacitor, Mica, 820 pf, 5%, 500 V, CM06E821J03	22047	2
	C75	· · Capacitor, Ceramic, 1.0 µf, +2%, 50 V	21748	1
	C76	· · Capacitor, Mica, 82 pf, 2%, 500 V, CM05E820G03	22108	1
	C77	· · Capacitor, Mica, 330 pf, 2%, 500 V, CM05E331G03	22117	1
	C84, C85	· · Not Used		
	CR1	· · Diode, 1N4001	35525	1
	CR2, CR3, CR5	· · Diode, 1N916	35514	3
	CR4	· · Diode, KV634 (MV1634)	29013	1

Table 6-11. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	CR6, CR7	· · Diode, KV650 (MV1650)	29006	2
	J1-J4,	· · Connector, SMB, Push-on	60044	7
	J5	· · Connector, 26-Pin, Rt. Angle, Control/Power	61228	1
	J6,J8-J9	· · Not Used		
	L1	· · Inductor, RF, 100μH, 10%, M890538-12	43033	1
	L2	· · Inductor, RF, 1μH, 10% M818130-8	43024	1
	L3, L5	· · Inductor, RF, 33μH, 10%	43031	2
	L4	· · Inductor, Variable	08525	1
	L6	· · Inductor, RF, 220μH, 10%, M890538-20	43027	1
	L7, L8	· · Inductor, RF, 5.6μH, 10%, M814046-1	43034	1
	L9, L10	· · Inductor, Variable	08522	2
	Q1-Q6, Q10, Q11, Q20	· · Transistor, NPN, 2N2369	32255	9
	Q7, Q9, Q15,Q17	· · Transistor, NPN, Audio, 2N3904	32036	4
	Q8, Q16	· · Transistor, PNP, Audio, 2N4126	31508	2
	Q18, Q19	· · Transistor, FET, RF, 2N4416A	32524	2
	Q22	· · Transistor, NPN, Power, 2N4921	32039	1
	Q12, Q13, Q14, Q21	· · Not Used		
	R1, R15, R16, R17, R30, R31, R71, R79, R80-R82, R70	· · Not Used		

Table 6-11. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R2	• • Resistor, Film, 1 ohm, 5%, 1/4 W	12153	1
	R3	• • Resistor, Film, 3.9 K, 2%, 1/4 W	12161-392	1
	R4	• • Resistor, Film, 6.8 K, 2%, 1/4 W	12161-682	1
	R5, R39, R60, R64	• • Resistor, Film, 2.2 K, 2%, 1/4 W	12161-22	4
	R6, R33, R34, R38, R59, R63, R67,	• • Resistor, Film, 680 ohm, 2%, 1/4 W	12161-681	7
	R7, R24, R25, R72	• • Resistor, Film, 4.7 K, 2%, 1/4 W	12161-472	4
	R8, R14 R32, R83, R56	• • Resistor, Film, 47 ohms, 2%, 1/4 W	12161-470	5
	R9	• • Resistor, Film, 33 ohms, 2%, 1/4 W	12161-330	1
	R10, R13, R23, R41, R43-R45, R48, R49, R54, R57, R58, R74, R84	• • Resistor, Film, 1.0 K 2%, 1/4 W	12161-102	14
	R11, R27, R69	• • Resistor, Film, 330 ohms, 2%, 1/4 W	12161-331	3
	R12, R26,	• • Resistor, Film, 10 ohms, 2%,	12161-100	2
	R18, R20, R37, R62	• • Resistor, Film, 3.3 K, 2%, 1/4 W	12161-332	4
	R19, R21, R75	• • Resistor, Film, 1.8 K , 2%, 1/4 W	12161-182	3
	R22, R35, R76, R77	• • Resistor, Film, 820 ohms, 2%, 1/4 W	12161-821	4
	R28, R29, R36, R47,	• • Resistor, Film, 10 K, 2%, 1/4 W	12161-103	7

Table 6-11. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R61, R73, R78	· · (Cont.)		
	R40, R42, R50, R41, R55	· · Resistor, Film, 470 ohms, 2%, 1/4 W	12161-471	5
	R46	· · Resistor, Film, 56 ohms, 2%, 1/4 W	12161-560	1
	R52	· · Resistor, Film, 220 ohms, 2%, 1/4 W	12161-221	1
	R53	· · Resistor, Film, 100 ohms, 2%, 1/4 W	12161-101	1
	R65	· · Resistor, Film, 18 K, 2%, 1/2 W	12161-183	1
	R66, R68	· · Resistor, Film, 560 K, 2%, 1/4 W	12161-564	2
	U1	· · Integrated Circuit, uA723PC, Voltage Regulator	36728	1
	U2	· · Integrated Circuit, 74LS00, Quad, 2 1/P, NAND	36632	1
	U3, U7	· · Integrated Circuit, 74LS74, Dual 'D' Flip Flop	36636	2
	U4, U5	· · Integrated Circuit, 74LS151, Data Selector	36743	2
	U6	· · Integrated Circuit, 74LS90, Decade Counter	36637	1
	U8, U9, U20	· · Integrated Circuit, 74LS390, Dual Decade Counter	36744	3
	U10	· · Integrated Circuit, MS38510/30102BCA	36884	1
	U11	· · Integrated Circuit, DM74LS00, National Only	36809	1
	U12	· · Integrated Circuit, 74LS02, Quad, 2-NOR	36660	1
	U13	· · Integrated Circuit, 74LS08, Quad, 2-AND	36734	1

Table 6-11. 2nd LO/BFO Synthesizer Circuit Card Assembly (A8)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	U14-U18	· · Integrated Circuit, 74LS160, Synchronous, 4-Bit, Counter	36702	5
	U13	· · Integrated Circuit, 74LS08, Quad, 2-AND	36734	1
	U14-U18	· · Integrated Circuit, 74LS160, Synchronous, 4-Bit, Counter	36702	5
	U19	· · Integrated Circuit, 11C90--10/11 Prescaler	36745	1
	U21	· · Not Used		
	U22	· · Integrated Circuit, 10115, ECL, Line Receiver	36805	1
	Y1	· · Oscillator, TCXO	08289	1
	Y2	· · Oscillator, Crystal, 20 MHz (CR78/U)	37039	1
		· · Tubing, PTFE #24*	59538	1
		· · Wire, #24*	58007	1
		· · Transistor Pad (Ref. Q1-Q6, Q10, Q11, Q18, Q19, Q20)*	70752	11
		· · Insulator, Mica, Round, I.D. .130, O.D. .50*	70793	1
		· · Thermal Compound, Type 128 or Eq.*	91012	1
		· · Washer, Flat, #4*	75022	2
		· · Washer, Split Lock, #4*	75002	1
		· · Screw, Pan Head, #4-40x15/16" Lg.*	76013	1
		· · Nut, Hex, #4*	75203	1
		· · Ceramic Beads*	70854	6
		· · Terminal*	70028	16

*NOTE: These components are not shown on illustration.

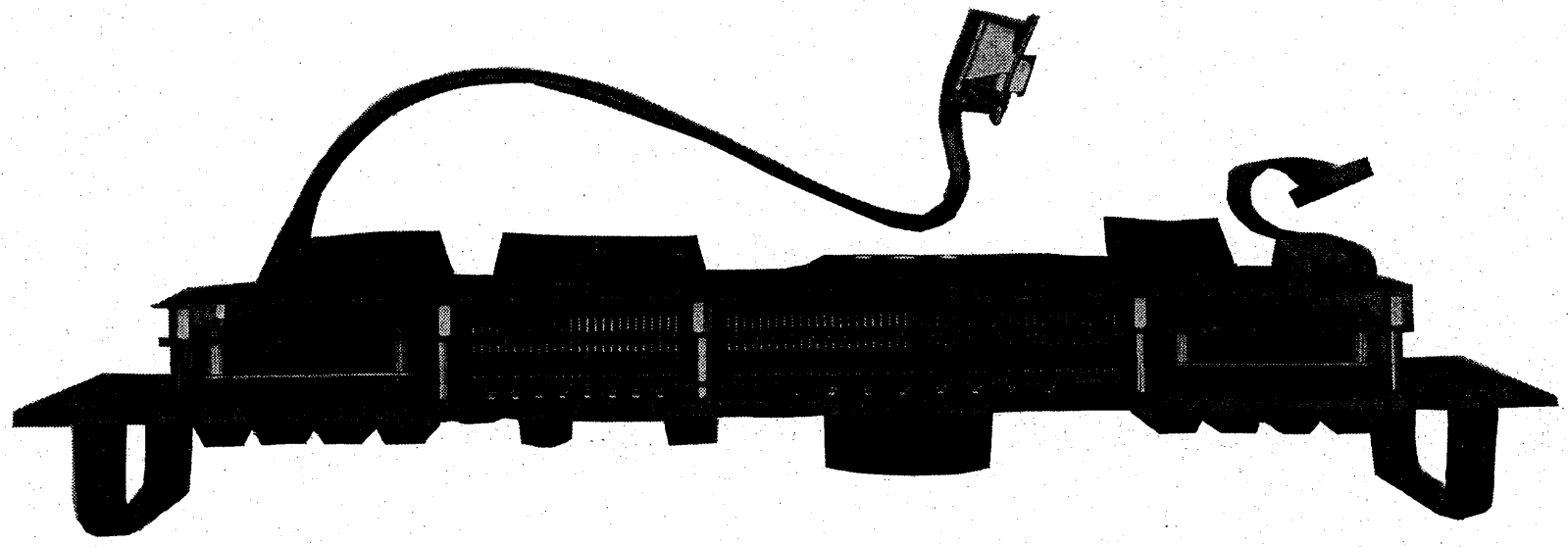


Figure 6-15. Receiver Control Circuit Card Assembly (A9)

Table 6-12. Front Panel Assembly (A9)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A9	Front Panel Assembly (Interconnecting Wiring Diagram 09024)	4100102-501	1
	A1	· Switch/Display Circuit Card Assembly (Schematic No. 4200010)	A08950-4	1
	A2	· Receiver Control Circuit Card Assembly (Schematic No. 08953)	A08952	1
	A3	· LCD/LED Circuit Card Assembly (Schematic No. 09482)	A09481-2	1
	J4	· Connector, Phone Jack, JJ-034	61502	1
	R1	· Resistor, Variable, 50 K, IF Gain	08552	1
	R2	· Resistor, Variable, 25 K, AF Gain	08551	1
	S1	· Switch, Toggle, Min. DPDT (p/o W20) C-M-JMT 223	52424	1
	W20	· Cable, AC Line Switching	08570	1

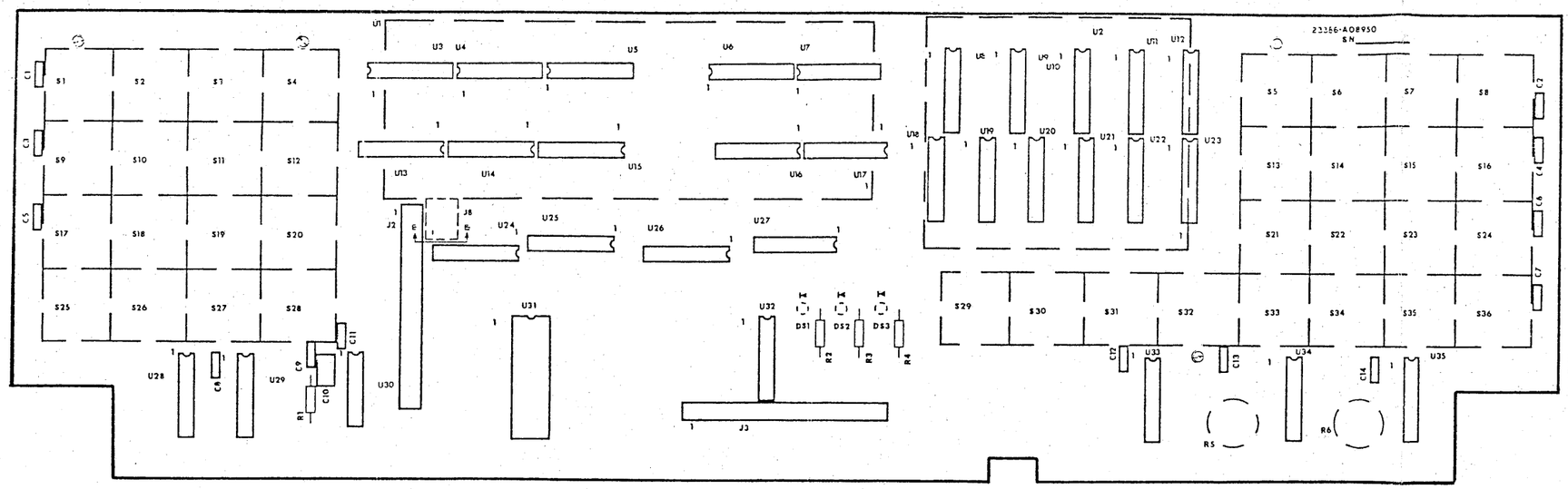


Figure 6-16. Switch/Display Circuit Card Assembly (A9A1) Component Location Diagram

Table 6-13. Switch/Display Circuit Card Assembly (A9A1) Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A9A1	Switch/Display Circuit Card Assembly (Schematic No. 4200010)	A08950-4	1
		· Printed Circuit Card Wiring Assembly	E08841	1
	C1-C9, C11-C14	· · Capacitor, Ceramic, 0.01 µf, ±20%, Erie Redcap 8121-050-651-103M	21733	13
	C10	· · Capacitor, Ceramic, 0.1 µf, ±20% Erie Redcap 8131-050-651-104M	21732	1
	DS1	· · Display, LED, Red, T1 Hewlett Packard, HLMP-1300	41030	1
	DS2	· · Display, LED, Yellow, T1 Hewlett Packard HLMP-1400	41031	1
	DS3	· · Display, LED, Green, T1 Hewlett Packard HLMP-1500	41032	1
	J2, J3	· · Connector, Bergstik, 20-Pin	61304	2
	J8	· · Connector, 4-Contact, Rt. Angle Bergstik	08573	1
	R1	· · Resistor, Film, 15 K, ±2%, 1/4 W	12161-153	1
	R2-R4	· · Resistor, Film, 330 ohm, ±2%, 1/4 W	12161-331	1
	R5, R6	· · Resistor, Variable 25 K	08473	2
	S1-S36	· · Switch, Pushbutton, Module, Microswitch 1001SD4A3A	52419	36
	U1	· · LCD, Frequency/Channel, SR-410 Crystaloid	08725	1
	U2	· · LCD, Display, Multi-Descriptive	08526	1
	U3-U9, U13-U17, U25-U27	· · Integrated Circuit, 4056	36752	15
	U10-U12, U18-U24	· · Integrated Circuit, 4054	36750	10
	U28, U29, U33-U35	· · Integrated Circuit, 4051	36687	5

Table 6-13. Switch/Display Circuit Card Assembly (A9A1)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	U30	· · Integrated Circuit, 4047	36786	1
	U31	· · Integrated Circuit, 4514	36751	1
	U32	· · Integrated Cjrcuit, 4028	36575	1
		· · Socket, SIP, 14-Contact	61298	4
		· · Socket, SIP, 12-Contact	61297	6
		· · Socket, SIP, 11-Contact	61296	1
	S19	· · Key-Switch, Pushbutton, Mkg. (1)	08671-1	1
	S18	· · Key-Switch, Pushbutton, Mkg. (2)	08671-2	1
	S17	· · Key-Switch, Pushbutton, Mkg. (3)	08671-3	1
	S11	· · Key-Switch, Pushbutton, Mkg. (4)	08671-4	1
	S10	· · Key-Switch, Pushbutton, Mkg. (5)	08671-5	1
	S9	· · Key-Switch, Pushbutton, Mkg. (6)	08671-6	1
	S3	· · Key-Switch, Pushbutton, Mkg. (7)	08671-7	1
	S1	· · Key-Switch, Pushbutton, Mkg. (9)	08671-9	1
	S2	· · Key-Switch, Pushbutton, Mkg. (8)	08761-8	1
	S26	· · Key-Switch, Pushbutton, Mkg. (0)	08671-10	1
	S25	· · Key-Switch, Pushbutton, Mkg. (LOCAL RMTE)	08671-34	1
	S27	· · Key-Switch, Pushbutton, Mkg. (ENTER)	08671-35	1
	S20	· · Key-Switch, Pushbutton, Mkg. (BFO VAR)	08671-36	1
	S32	· · Key-Switch, Pushbutton, Mkg. (STORE)	08671-45	1
	S4	· · Key-Switch, Pushbutton, Mkg. (TUNE RATE)	08671-55	1
	S16	· · Key-Switch, Pushbutton, Mkg. (ISB U/L)	08671-57	1
	S8	· · Key-Switch, Pushbutton, Mkg. (AM)	08671-58	1
	S7	· · Key-Switch, Pushbutton, Mkg. (CW)	08671-59	1
	S6	· · Key-Switch, Pushbutton, Mkg. (USB)	08671-60	1
	S5	· · Key-Switch, Pushbutton, Mkg. (LSB)	08671-61	1
	S21	· · Key-Switch, Pushbutton, Mkg. (LONG)	08671-68	1
	S22	· · Key-Switch, Pushbutton, Mkg. (MED)	08671-74	1
	S23	· · Key-Switch, Pushbutton, Mkg. (SHORT)	08671-67	1

Table 6-13. Switch/Display Circuit Card Assembly (A9A1)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	S24	· · Key-Switch, Pushbutton, Mkg. (MAN)	08671-73	1
	S12	· · Key-Switch, Pushbutton, Mkg. (LOCK/2ND)	08671-80	1
	S34	· · Key-Switch, Pushbutton, Mkg. (SWEEP)	08671-79	1
	S33	· · Key-Switch, Pushbutton, Mkg. (THLD)	08671-78	1
	S36	· · Key-Switch, Pushbutton, Mkg. (BW)	08671-29	1
	S13	· · Key-Switch, Pushbutton, Mkg. (DIG RF)	08671-82	1
	S28	· · Key-Switch, Pushbutton, Mkg. (BFCNT/SCCLR)	08671-83	1
	S29	· · Key-Switch, Pushbutton, Mkg. (CONT/STOP)	08671-81	1
	S30	· · Key-Switch, Pushbutton, Mkg. (LOAD)	08671-21	1
	S14	· · Key-Switch, Pushbutton, Mkg. (METER RF/AF)	08671-70	1
	S35	· · Key-Switch, Pushbutton, Mkg. (SCAN)	08671-52	1
	S31	· · Key-Switch, Pushbutton, Mkg. (CHAN)	08671-69	1
		· · Knob, Modified (Encoder)*	B08557	1
		· · Knob (R1 & R2)*	81042	2
		· · Handle*	81796	2
		· · Retainer, Ring*	75116	1
		· · Bushing, Spacer (Encoder)*	B08196	1
		· · Shaft, Encoder, (Ref. 0.25" Dia.)*	B08934	1
		· · D c, Encoder (Ref. 3.125" Dia.)*	B08194	1
		· · Nut, 1/2 - 20 Thd. Hex.*	75461	2
		· · Washer, Spring, 1/2" I.D.*	75129	2
		· · Washer, Shim, 1/4" I.D.*	75100	1

*NOTE: These components are not shown on illustration.

Table 6-13. Switch/Display Circuit Card Assembly (A9A1) Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
		• • Washer, Flat, 1/2" I.D.*	75131	2
		• • Washer, Flat, 1/4" I.D.*	75106	2
		• • Washer, Sprint, 1/4" I.D.*	75133	1
		• • Washer, Nylon, 1/2" I.D.* (.503 x 1.002 x .032 Thk.)	75132	2
		• • Stand-Off, Male/Female* #4-40, 0.75" Lg.	SP03-106	12
		• • Stand-Off, Female/Female* 4-40 0.375" Long	SP01-017	12
		• • Screw, Flat Head, #10-32*	76772	4
		• • Washer, Spring #4*	75112	12
		• • Washer, 3/8" Int. Tooth*	75074	2
		• • Nut 3/8-32*	75433	2
		• • Screw, #4-40 x 5/16" Lg.*	76013	13
		• • Washer, Flat #4*	75022	15
		• • Washer, Split Lock #4*	75002	15
		• • Light Defuser*	C09982	1
		• • Cable, DC Power to LCD/LED*	B09492-2	1
		• • Wire, #24 Black*	55097	1
		• • Wire, #24 White*	55096	1
		• • Wire, #24 White/Green*	55108	1
		• • Wire, #24 Green*	55099	1
		• • Wire, #24 Yellow*	55100	1
		• • Wire, #24 Blue*	55101	1
		• • Wire, #24 White/Blue*	55110	1
		• • Nut, Hex, 4-40*	75203	2

*NOTE: These components are not shown on illustration.

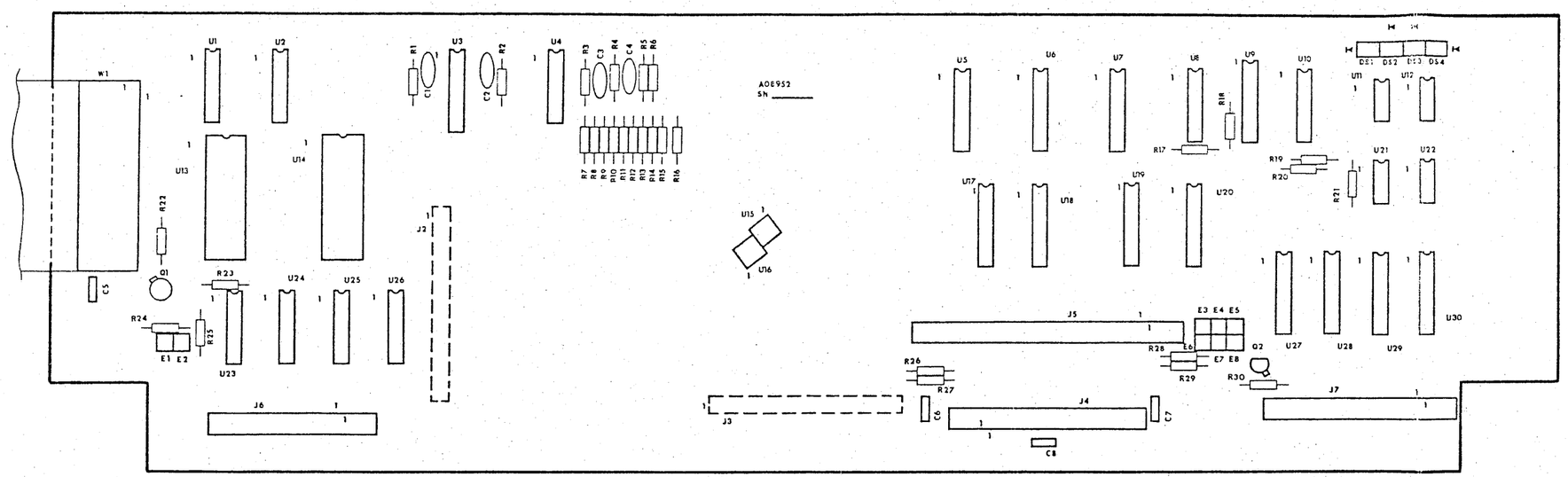


Figure 6-17. Receiver Control Circuit Card Assembly (A9A2) Component Location Diagram

Table 6-14. Receiver Control Circuit Card Assembly (A9A2)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A9A2	Receiver Control Circuit Card Assembly (Schematic No. 08953)	A08952	1
		· Printed Circuit Card Wiring Assembly	08916	1
	C1, C2	· · Capacitor, Ceramic, 20 pf, ±5% Erie 801-000-C0G0-200J	21352	2
	C3, C4	· · Capacitor, Ceramic, 100 pf, ±10%, Erie 831-000-X5F0-100K	21763	2
	C5	· · Capacitor, Ceramic, 0.01 µf, ±20%, Erie 8121-050-651-103M	21733	1
	C6-C8	· · Capacitor, Ceramic, 0.22 µf, ±20%, Erie 8121-050-651-224M	21742	3
	DS1-DS4	· · LED, Resistor Assembly HP HLMP 6620	41018	4
	J2, J3	· · Connector, 20-Contact, Single Row, Mod. IV, AMP 87334-8	61303	2
	J4, J7	· · Connector, 26-Contact, (BFO and POWER)	61231	2
	J5	· · Connector, 40-Contact, (A4 IF)	61230	1
	J6	· · Connector, 20-Contact, (A7 Synthesizer)	61213	1
	Q1	· · Transistor, 2N2369	32255	1
	Q2	· · Transistor, 2N3906	32037	1
	R1, R2	· · Resistor, Film, 33 K, ±2%, 1/4 W	12161-333	2
	R3, R4	· · Resistor, Film, 1 ohm, ±2%, 1/4 W	12161-105	2
	R5, R6, R23	· · Resistor, Film, 1 K, ±2%, 1/4 W	12161-102	3
	R7, R10, R26, R27	· · Resistor, Film, 3.9 K, ±2%, 1/4 W	12161-392	4
	R8, R9	· · Resistor, Film, 11 K, ±2%, 1/4 W	12161-113	2
	R11, R12	· · Resistor, Film, 100 K, ±2%, 1/4 W	12161-104	2
	R13, R14, R17-R21	· · Resistor, Film, 22 K, ±2%, 1/4 W	12161-223	7
	R15, R16	· · Resistor, Film, 180 ohm, ±2%, 1/4 W	12161-181	2

Table 6-14. Receiver Control Circuit Card Assembly (A9A2)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	R22, R25, R29, R30	· · Resistor, Film, 10 K, ±2%, 1/4 W	12161-103	4
	R24	· · Resistor, Film, 100 ohm, ±2%, 1/4 W	12161-101	1
	R28	· · Resistor, Film, 15 K, ±2%, 1/4 W	12161-153	1
	U1, U2	· · Integrated Circuit, 4066	36792	2
	U3	· · Integrated Circuit, 4528	36611	1
	U4	· · Integrated Circuit, LM339	36693	1
	U5	· · Integrated Circuit, 4516	36583	1
	U6	· · Integrated Circuit, 4051	36687	1
	U7, U18, U20	· · Integrated Circuit, 4503	36694	3
	U8, U10	· · Integrated Circuit, 4013	36588	2
	U9, U17, U19	· · Integrated Circuit, Resistor, Network, 8 Pin, SIP, 10 K	19321-103	3
	U11, U12, U21, U22	· · Integrated Circuit, 40107	36795	4
	U13	· · Integrated Circuit, 4508	36810	1
	U14	· · Integrated Circuit, 4514	36751	1
	U15, U16	· · Integrated Circuit, 0PB706A	36754	2
	U23, U25	· · Integrated Circuit, 4069	36685	2
	U24	· · Integrated Circuit, 4025	36649	1
	U26	· · Integrated Circuit, 4081	36677	1
	U27-U30	· · Integrated Circuit, 4099	36808	4
	W1	· · Cable Assembly	08536	1
		· · Transistor Pad (Ref. Q1)*	70752	1

*NOTE: These components are not shown on illustration.

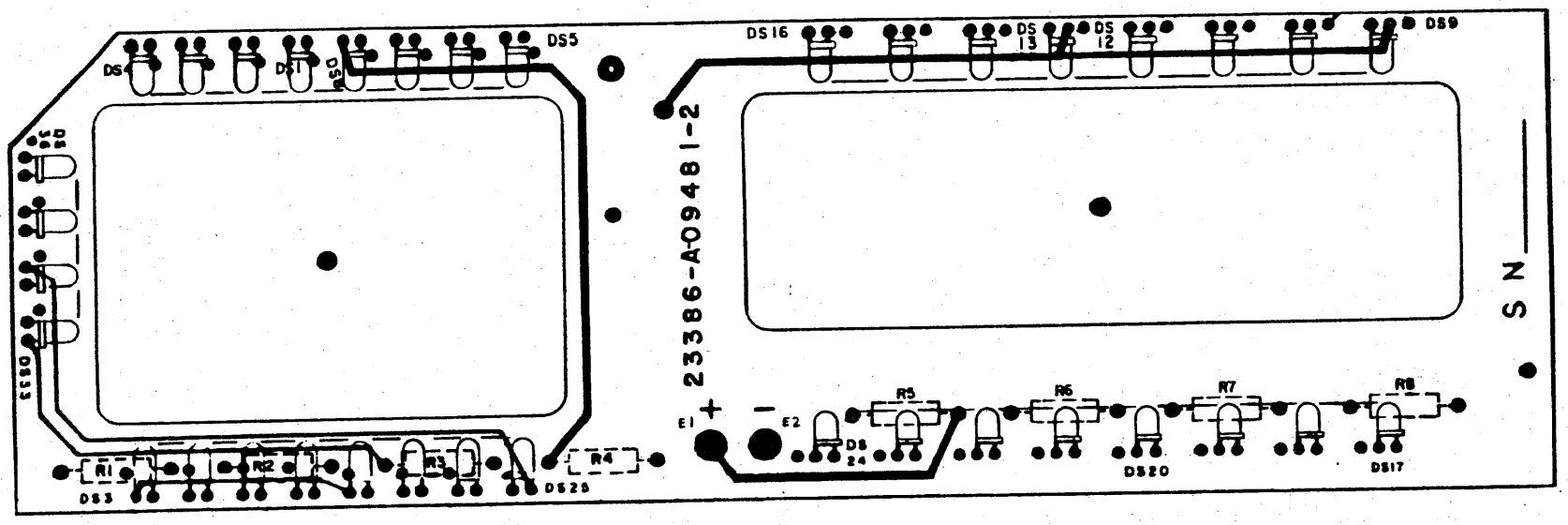


Figure 6-18. LCD/LED Circuit Card Assembly (A9A3)
Component Location Diagram

Table 6-15. LCD/LED Circuit Card Assembly (A9A3)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A9A3	LCD/LED Circuit Card Assembly (Schematic No. 09482)	09481-2	1
		· Printed Circuit Card Wiring Assembly	D09854	1
	DS1-DS36	· · LED Display	09806	36
	E1, E2	· · Terminal	70028	2
	R1, R3	· · Resistor, Fixed Comp. 62 ohm, 5%, 1/2 W	10934	2
	R2, R4, R5-R8	· · Resistor, Fixed, Comp., 180 ohm, 5%, 1/2 W	10945	6
	W1	· · Cable Assembly	09492-1	1

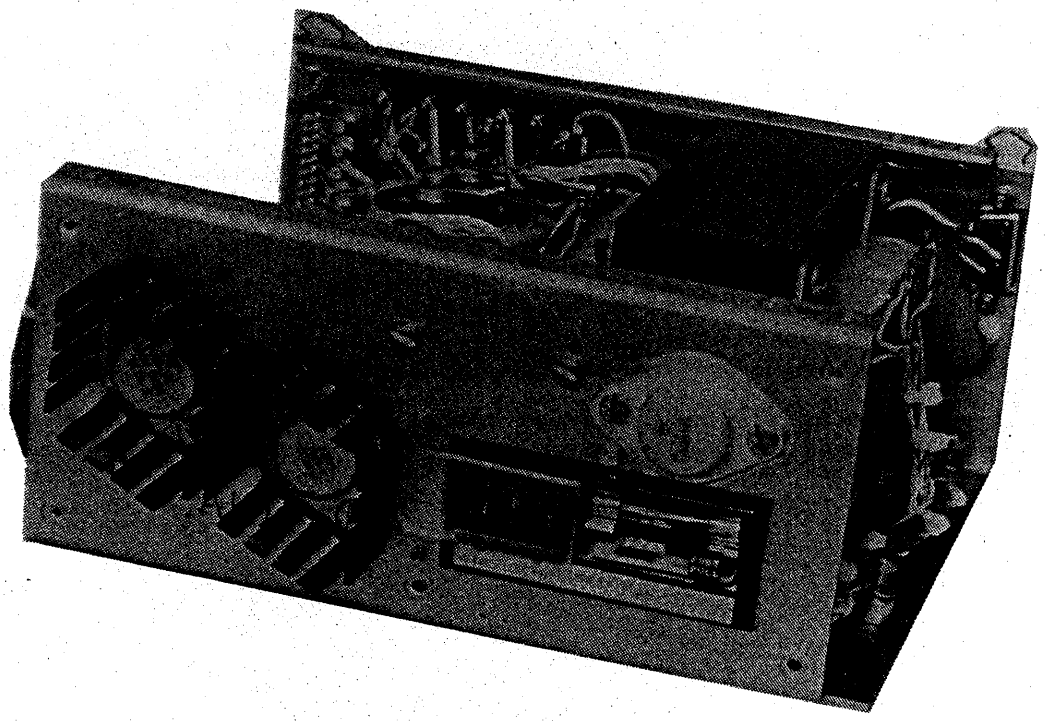


Figure 6-19. Power Supply Assembly, A10, Rear View

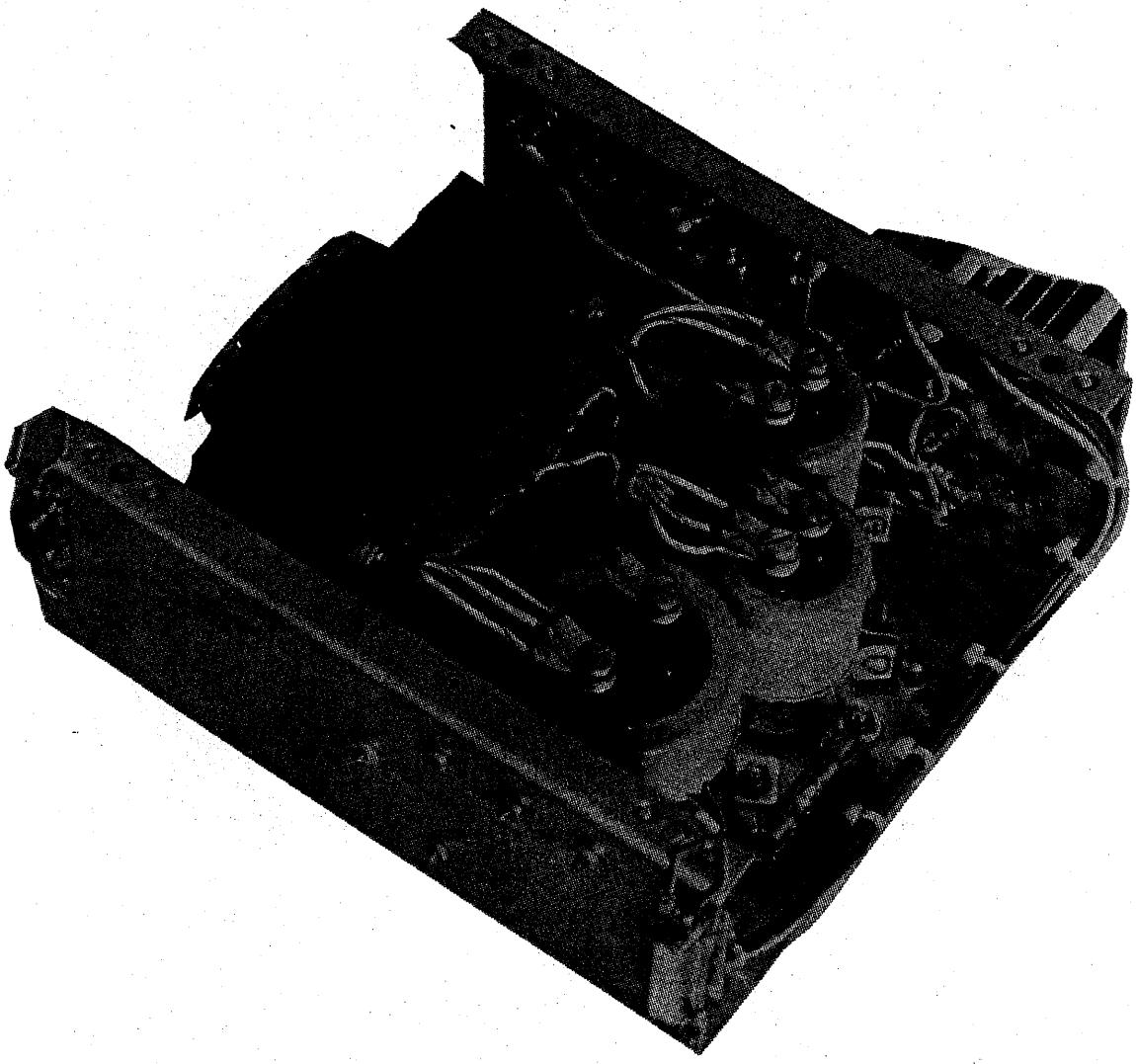
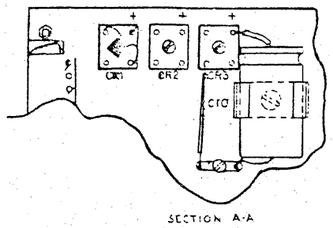


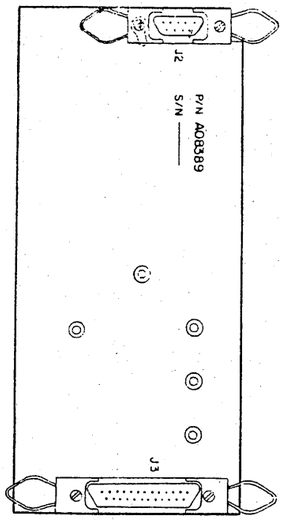
Figure 6-20. Power Supply Assembly, A10, Front View

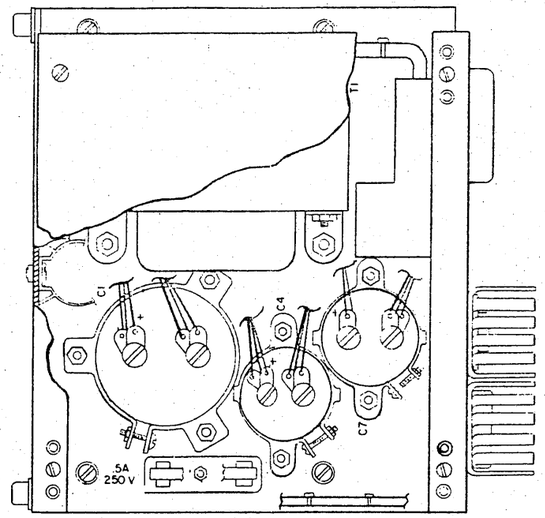
Table 6-16. Power Supply Module Assembly (A10)
Replacement Parts List

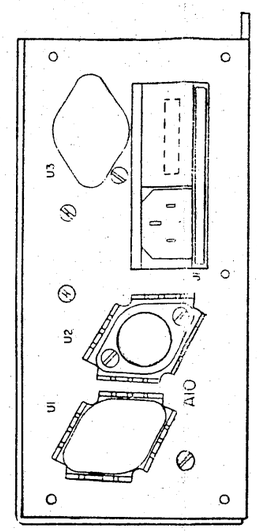
FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A10	Power Supply Assembly	08389	1
	A10A2	· +20 V Reg. Circuit Card Assembly	08593	1
	C1	· Capacitor, Electrolytic, 12500 µf, 25 V, -10 +75%	24063	1
	C2, C3, C5, C6, C8	· Capacitor, Tantalum, 1 µf, 35 V, ±20%	25068	5
	C4, C7	· Capacitor, Electrolytic, 5200 µf, 40 V, -10 +75%	24070	2
	C9	· Capacitor, Tantalum, 6.8 µf, 35 V, ±20%	25069	1
	C10	· Capacitor, Electrolytic, 1200 µf, 50 V, -10 +75%	24071	1
	C11	· Capacitor, Ceramic, 0.22 µf, 50 V, ±20%	21742	1
	CR1	· Diode, Rectifier	35561	1
	CR2-CR3	· Diode, Rectifier	35560	1
	F1	· Fuse, 1 amp., Slo-Blo, 125 V	40012	1
	J1	· Connector, Power Input, Filter and Fuse	61236	1
	J2	· Connector, AC, Switched Power	61166	1
	J3	· Power Supply Connector Assembly	08516-1	1
	R1	· Resistor, Metal Film, 33 ohms, ±2%, 1/4 W	12161-330	1
	T1	· Transformer, Power	08517	1
	U1	· Integrated Circuit, Regulator, +5 V, 5 amp.	36627	1
	U2	· Integrated Circuit, Regulator, +15 V, 1 amp.	36755	1
	U3	· Integrated Circuit, Regulator, -15 V, 1 amp.	36756	1

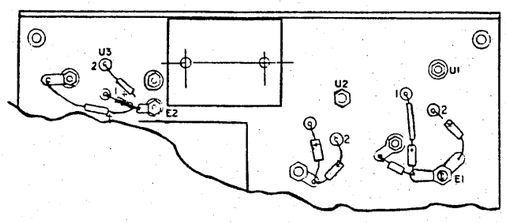


SECTION A-A









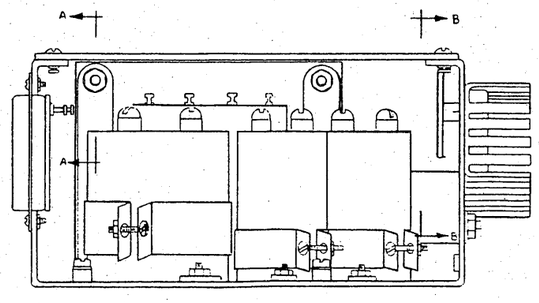


Figure 6-21. Power Supply Assembly (A10) Component Location Diagram

Table 6-16. Power Supply Module Assembly (A10)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	-	Fuse, 1/2 amp., Slo-Blo, 250 V, 3 AG	40028	1
	-	Fuseholder, Clip, Type, Spare for 220 V	40503	1
	-	Wiring Harness No. 1 A sembly	08513	1
	-	Wiring Harness No. 2 Assembly	08515	1

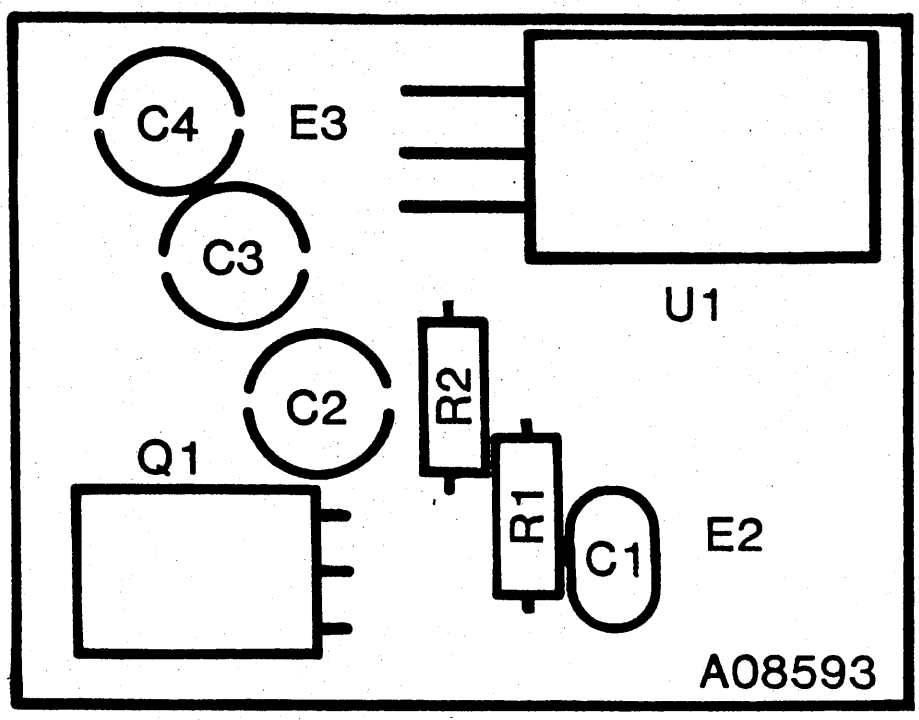


Figure 6-22. 20 Volt Regulator Assembly (A10A2)
Component Location Diagram (08593)

Table 6-17. 20 Volt Regulator Assembly (A10A2)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	RACAL PART NO.	QTY.
	A10A2	20 Volt Regulator Circuit Card Assembly	08593	1
	C1	· Capacitor, Ceramic, 0.01 µf, 50 V, ±20%	21733	1
	C2, C4	· Capacitor, Tantalum, 6.8 µf, 35 V, ±20%	25060-685	2
	C3	· Capacitor, Tantalum, 1 µf, 50 V, ±20%	25078-105	1
	Q1	· Transistor, Voltage Regulator	32519	1
	R1	· Resistor, Film, 4.7 K, ±2%, 1/4 W	12161-472	1
	R2	· Resistor, Film, 47 K, ±2%, 1/4 W	12161-473	1
	U1	· Integrated Circuit, +20 V DC Regulator	36819	1
	-	· Printed Circuit Card	08592	1

SECTION VII
SCHEMATIC DIAGRAMS

7.1 INTRODUCTION

Section VII contains circuit diagrams and interconnection diagrams applicable to the RA6793A HF Receiver. A listing of all diagrams, showing Figure number and Page number for each, is shown below for quick reference to any diagram.

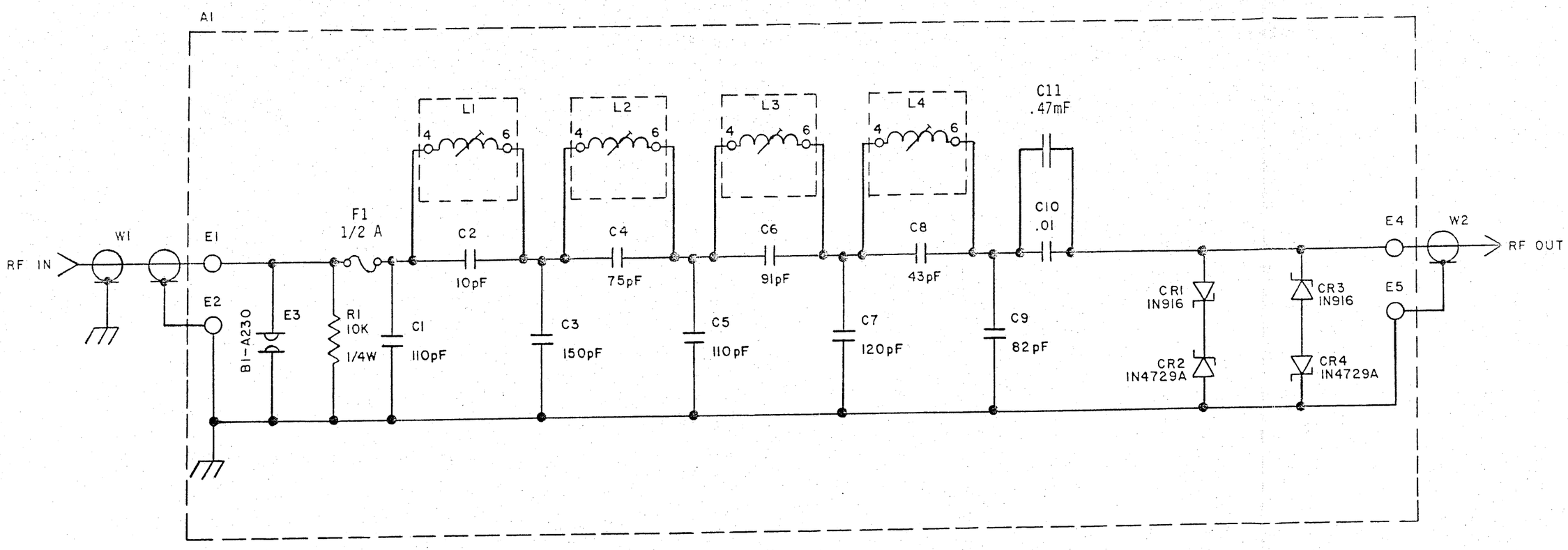
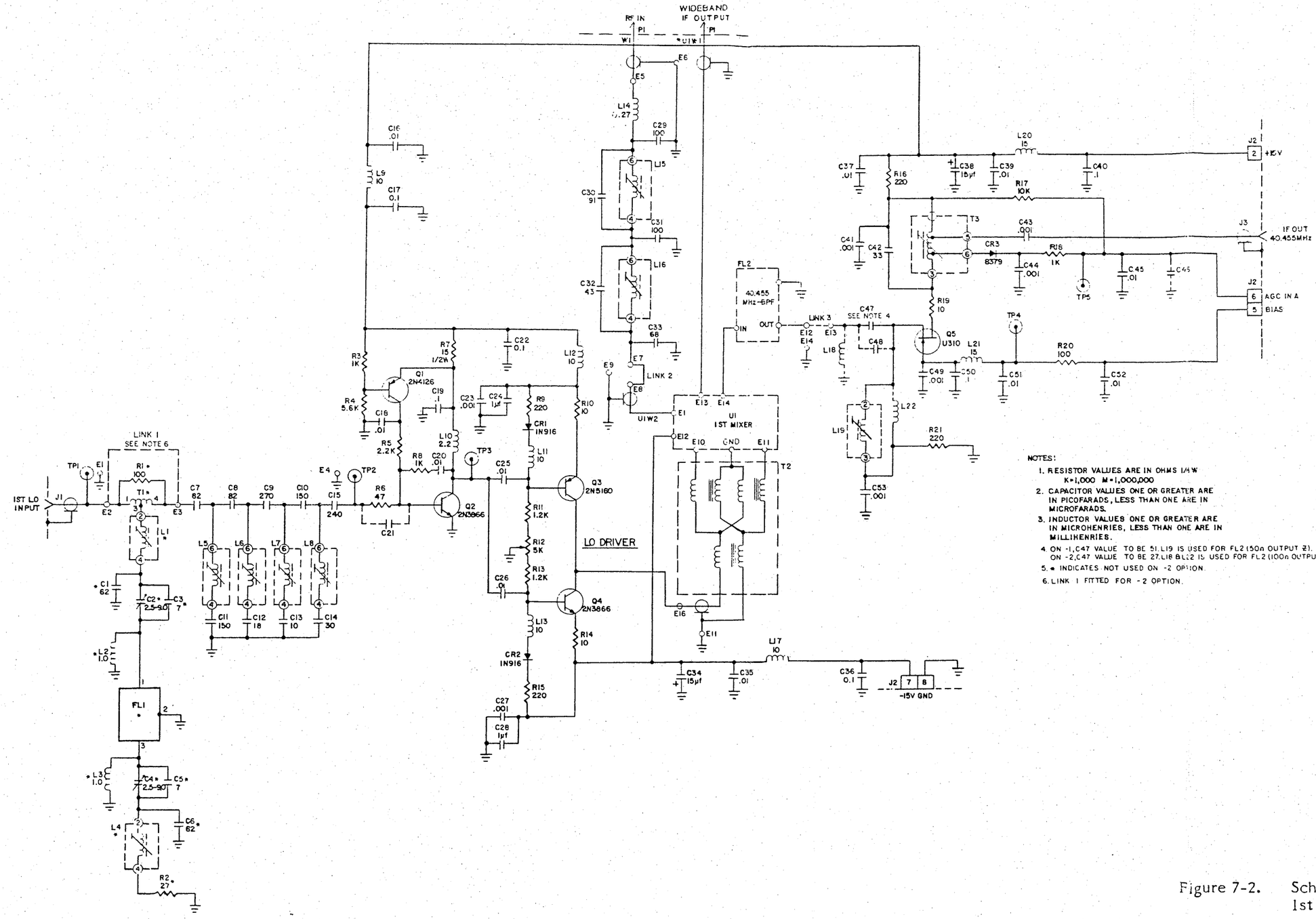


Figure 7-1. Schematic Diagram (09033), RF Low Pass Filter (A1A1)



NOTES:

1. RESISTOR VALUES ARE IN OHMS 1/4W
   K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTOR VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.
4. ON -1, C47 VALUE TO BE 51. L19 IS USED FOR FL2 (50Ω OUTPUT Z). ON -2, C47 VALUE TO BE 27. L18 & L22 IS USED FOR FL2 (100Ω OUTPUT Z)
5. * INDICATES NOT USED ON -2 OPTION.
6. LINK 1 FITTED FOR -2 OPTION.

Figure 7-2. Schematic Diagram (09018), 1st Mixer (A2)

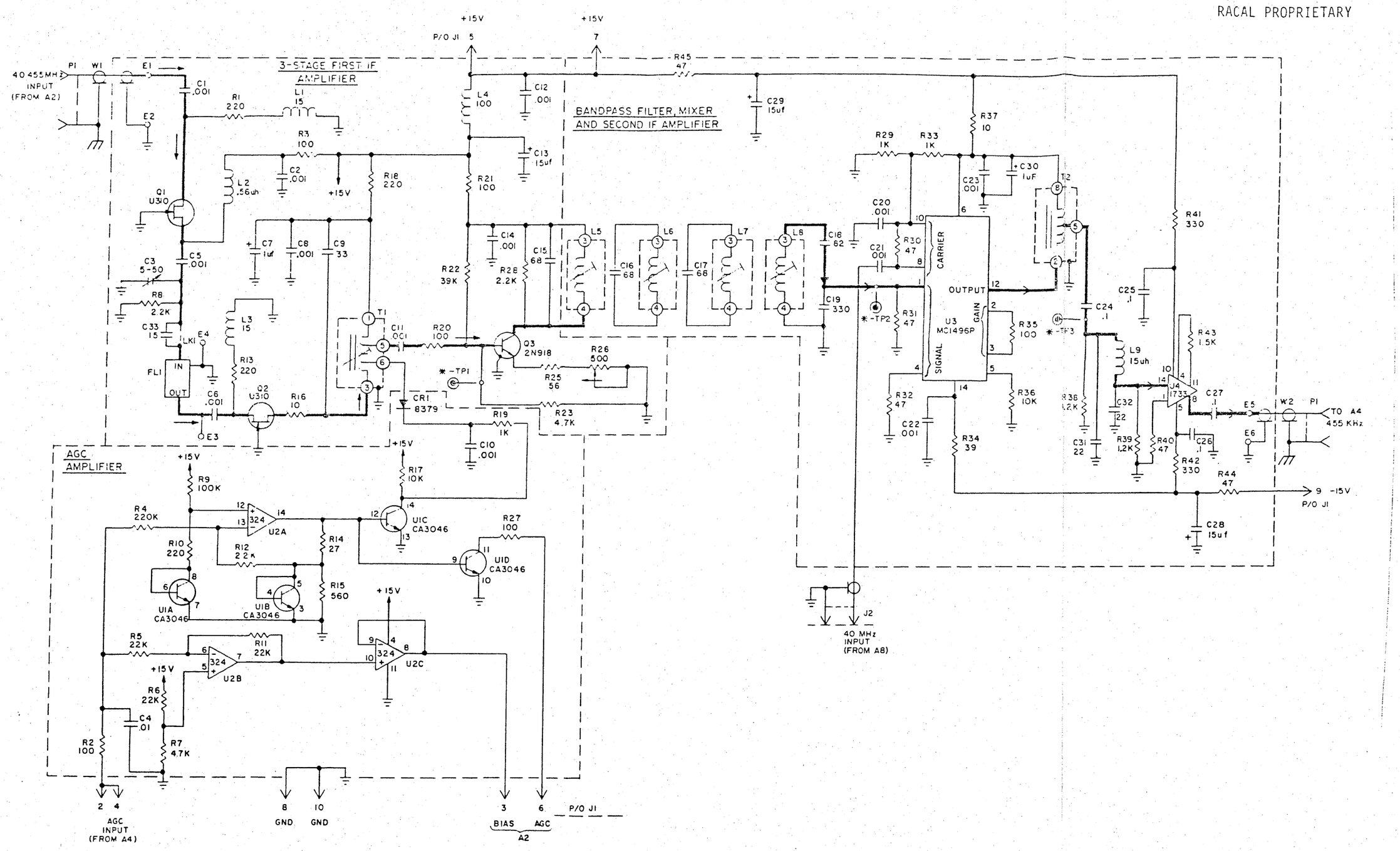


Figure 7-3. Schematic Diagram (08162), 2nd Mixer (A3)

SEE "A"

SEE "B"

Figure 7-4. Schematic Diagram (09664), Main IF/AF Converter (A4) (Sheet 1)

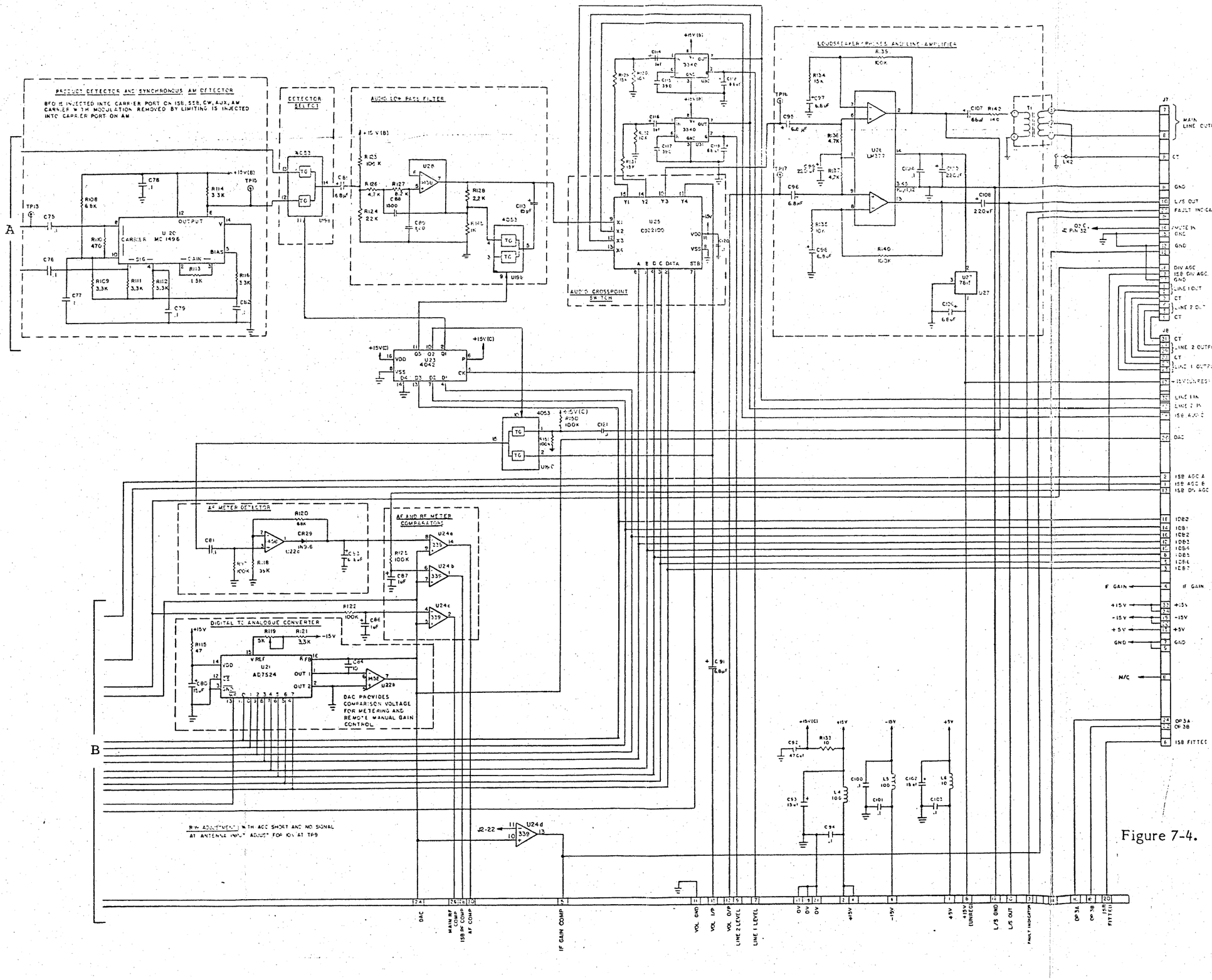
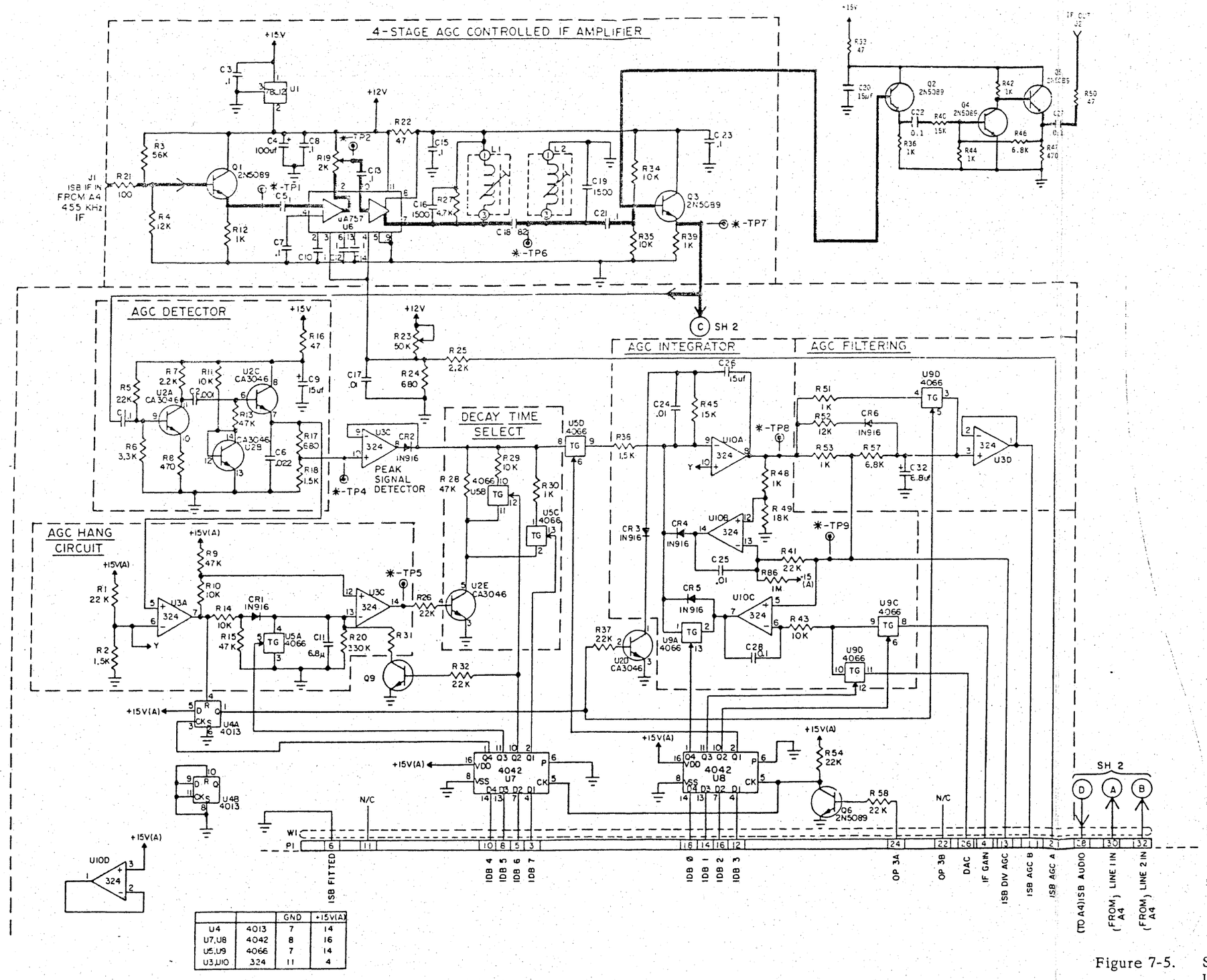


Figure 7-4. Schematic Diagram (09664), Main IF/AF Converter (A4) (Sheet 2)



		GND	+15V(A)
U4	4013	7	14
U7,U8	4042	8	16
U5,U9	4066	7	14
U3,U10	324	11	4

Figure 7-5. Schematic Diagram (08483) ISB (A5) (Optional) (Sheet 1)

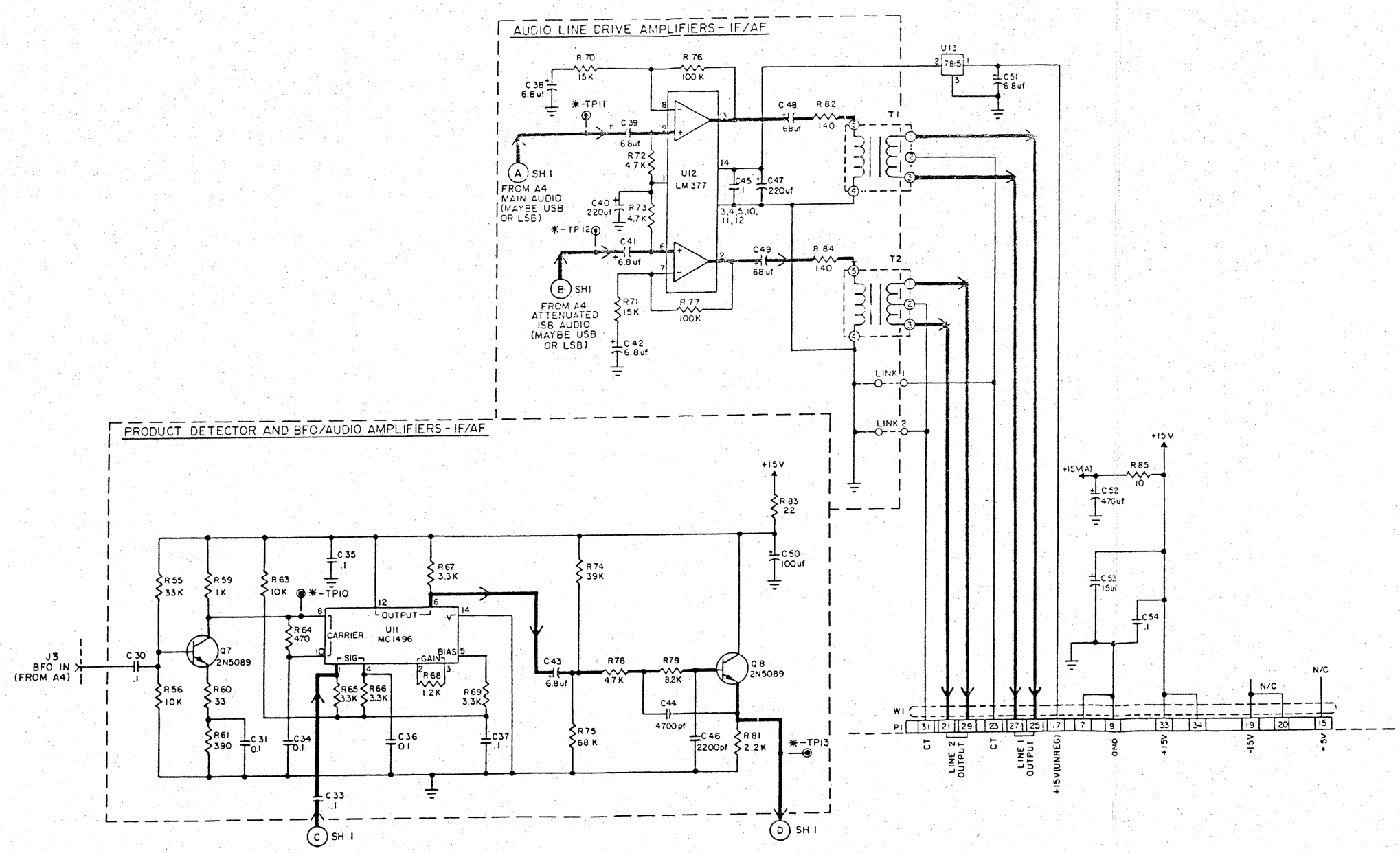


Figure 7-5. Schematic Diagram (08483), ISB (A5) (Optional) (Sheet 2)

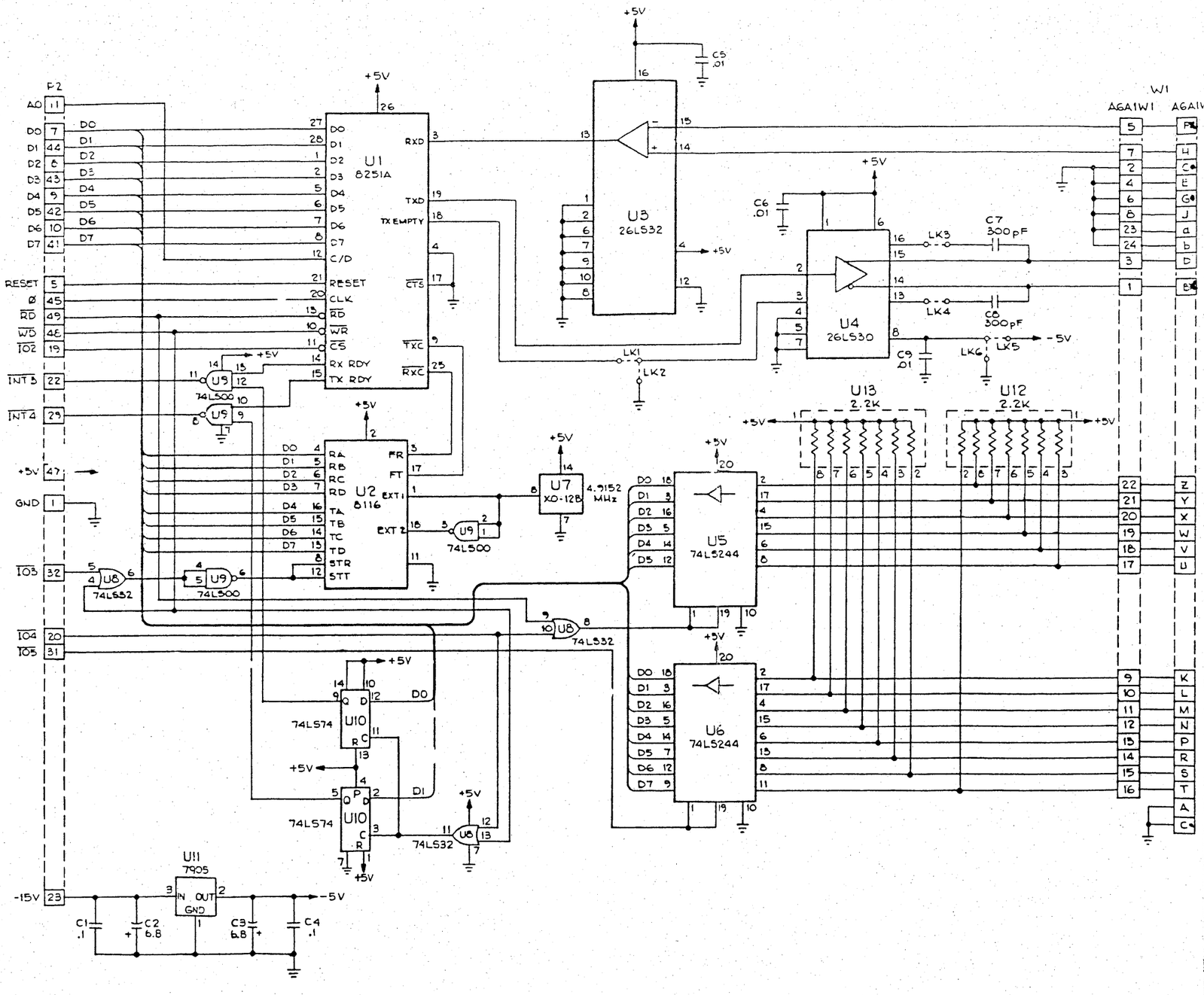


TABLE I

J1 PINS	FUNCTION
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND
F	DATA IN A
G	DATA IN GND
H	DATA IN B
J	GND
K	RECEIVER NUMBER D1-1
L	RECEIVER NUMBER D1-2
M	RECEIVER NUMBER D1-4
N	RECEIVER NUMBER D1-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

TABLE II DATA CONNECTION

J1 PINS	MS1880	RS232C RS423	RS422
A	SYSTEM GND	SYSTEM GND	SYSTEM GND
B	N.U.	DATA OUT A	DATA OUT A
C	DATA OUT GND	DATA OUT GND	N.U.
D	DATA OUT	N.U.	DATA OUT B
E	JUMPER TO 'F'	N.U.	N.U.
F	JUMPER TO 'E'	DATA IN A	DATA IN A
G	DATA IN GND	DATA IN GND	N.U.
H	DATA IN	JUMPER TO 'J'	DATA IN B
J	N.U.	JUMPER TO 'H'	N.U.

TABLE III
BAUD RATE SELECTION

DATA RATE SELECTION BIT				DATA RATE
W	X	Y	Z	(BAUD)
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

TABLE IV

LINK NO	1880C/232C/423	422
LK1	INSTALL	INSTALL
LK2	DELETE	DELETE
LK3	INSTALL	DELETE
LK4	INSTALL	DELETE
LK5	INSTALL	DELETE
LK6	DELETE	INSTALL

Figure 7-6. Schematic Diagram (09972), Asynchronous Interface (A6A1) (RS-232C Remote Control Interface)

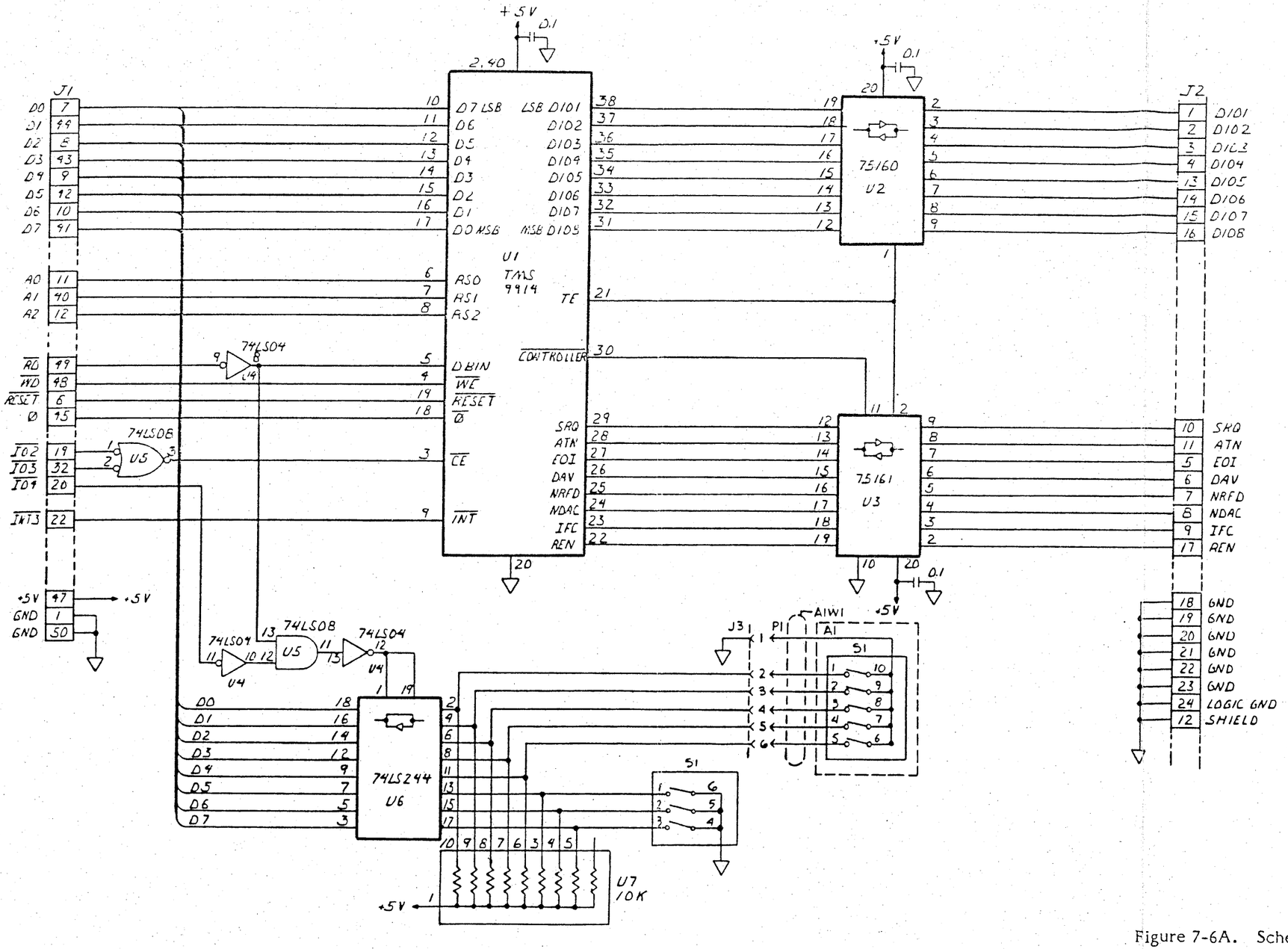


Figure 7-6A. Schematic Diagram (9850) Z80 GPI Interface (A6A1) (IEEE-488C Remote Control Interface)

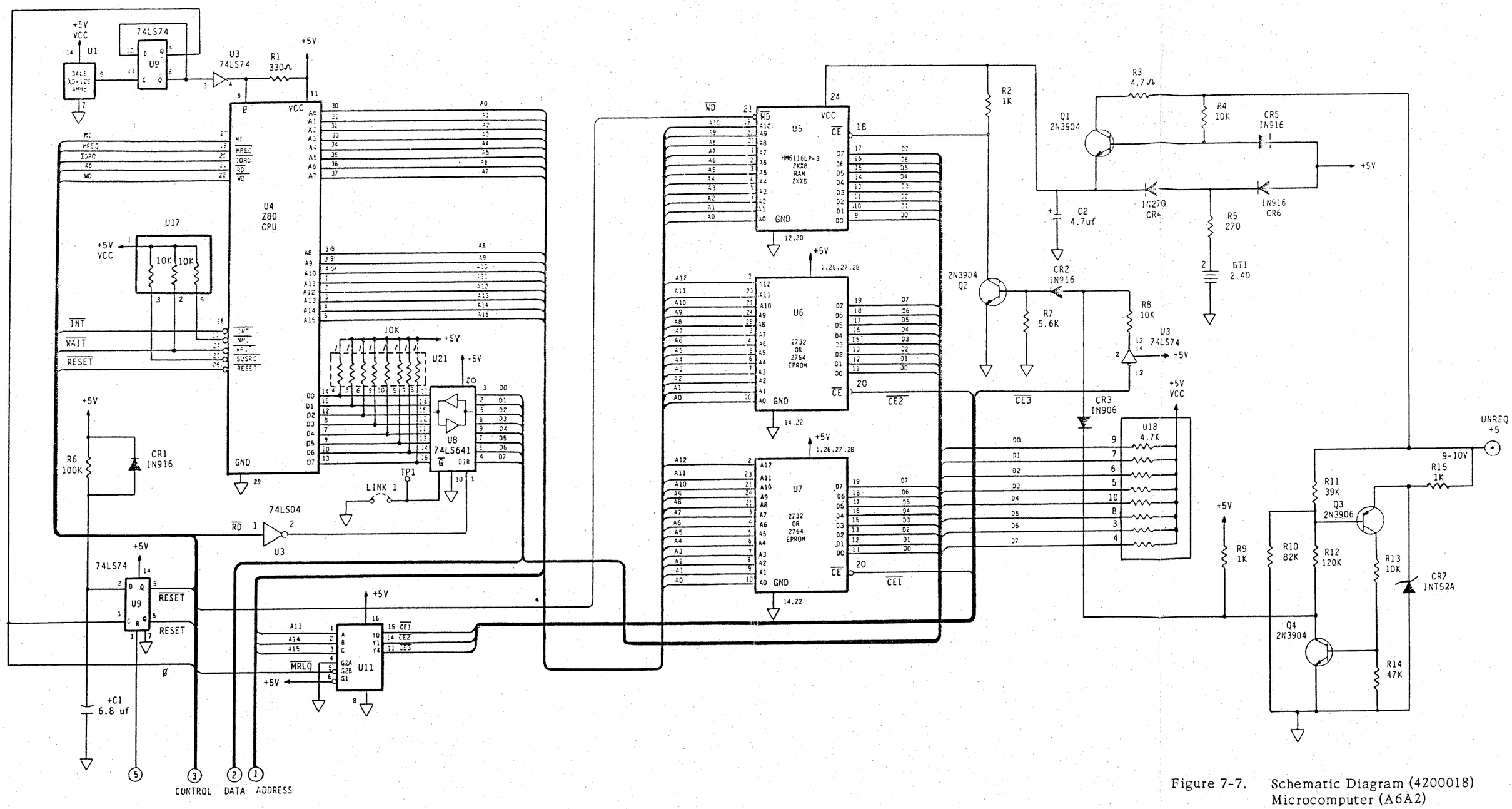
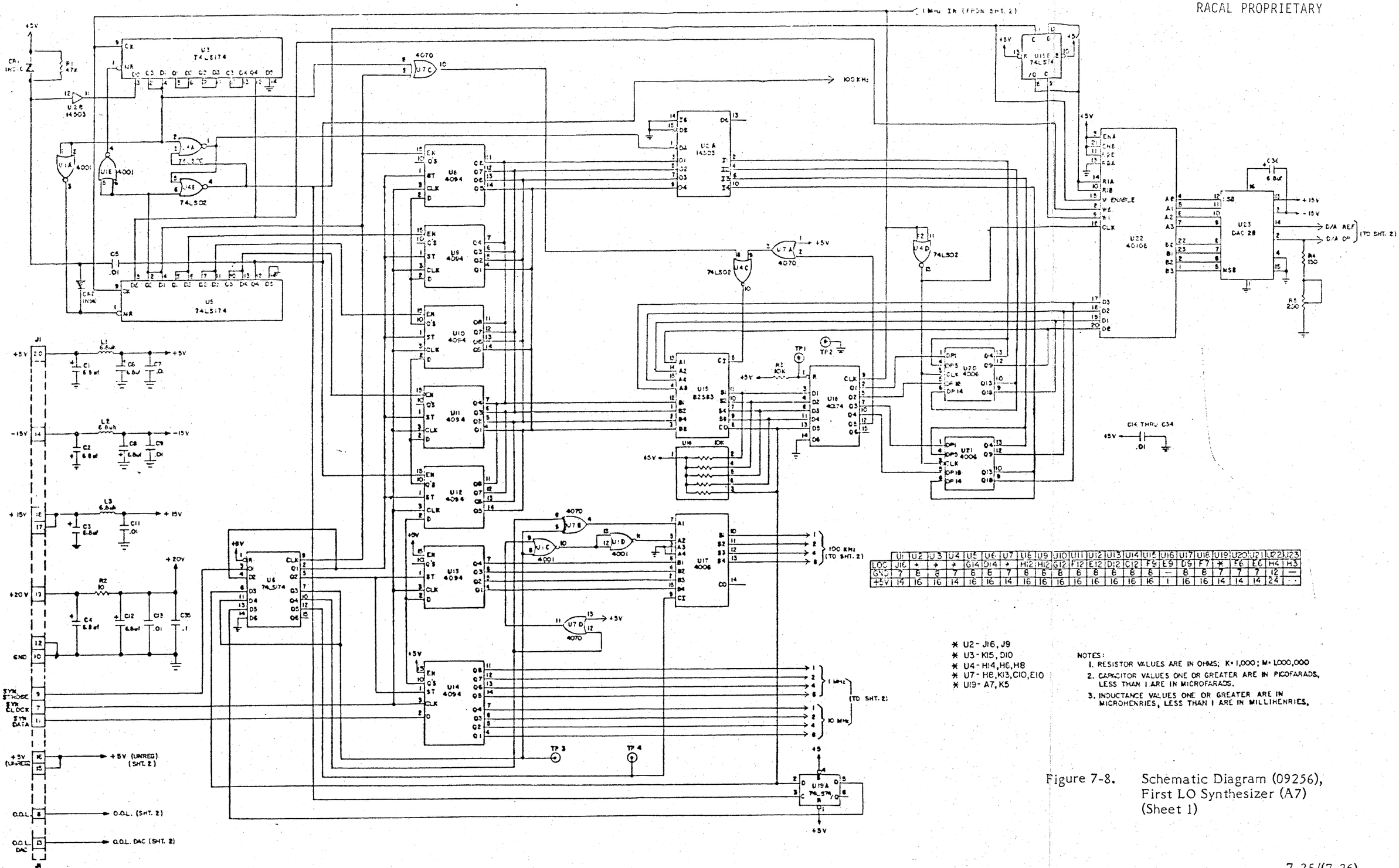


Figure 7-7. Schematic Diagram (4200018) Microcomputer (A6A2) (Sheet 1)

Figure 7-7. Schematic Diagram (4200018) Microcomputer (A6A2) (Sheet 2)



	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	LR2	U23
LOC	J16	→	→	→	G14	D14	→	H12	H12	G12	F12	E12	D12	C12	F9	E9	D9	F7	*	F6	E6	H4	H3
GND	7	8	8	7	8	8	7	8	8	8	8	8	8	8	8	—	8	8	7	7	7	12	—
+5V	14	16	16	14	16	16	14	16	16	16	16	16	16	16	16	1	16	16	14	14	14	24	-

* U2 - J16, J9
* U3 - K15, D10
* U4 - H14, H6, H8
* U7 - H8, K13, C10, E10
* U19 - A7, K5

NOTES:
1. RESISTOR VALUES ARE IN OHMS; K = 1,000; M = 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN 1 ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN 1 ARE IN MILLIHENRIES.

Figure 7-8. Schematic Diagram (09256), First LO Synthesizer (A7) (Sheet 1)

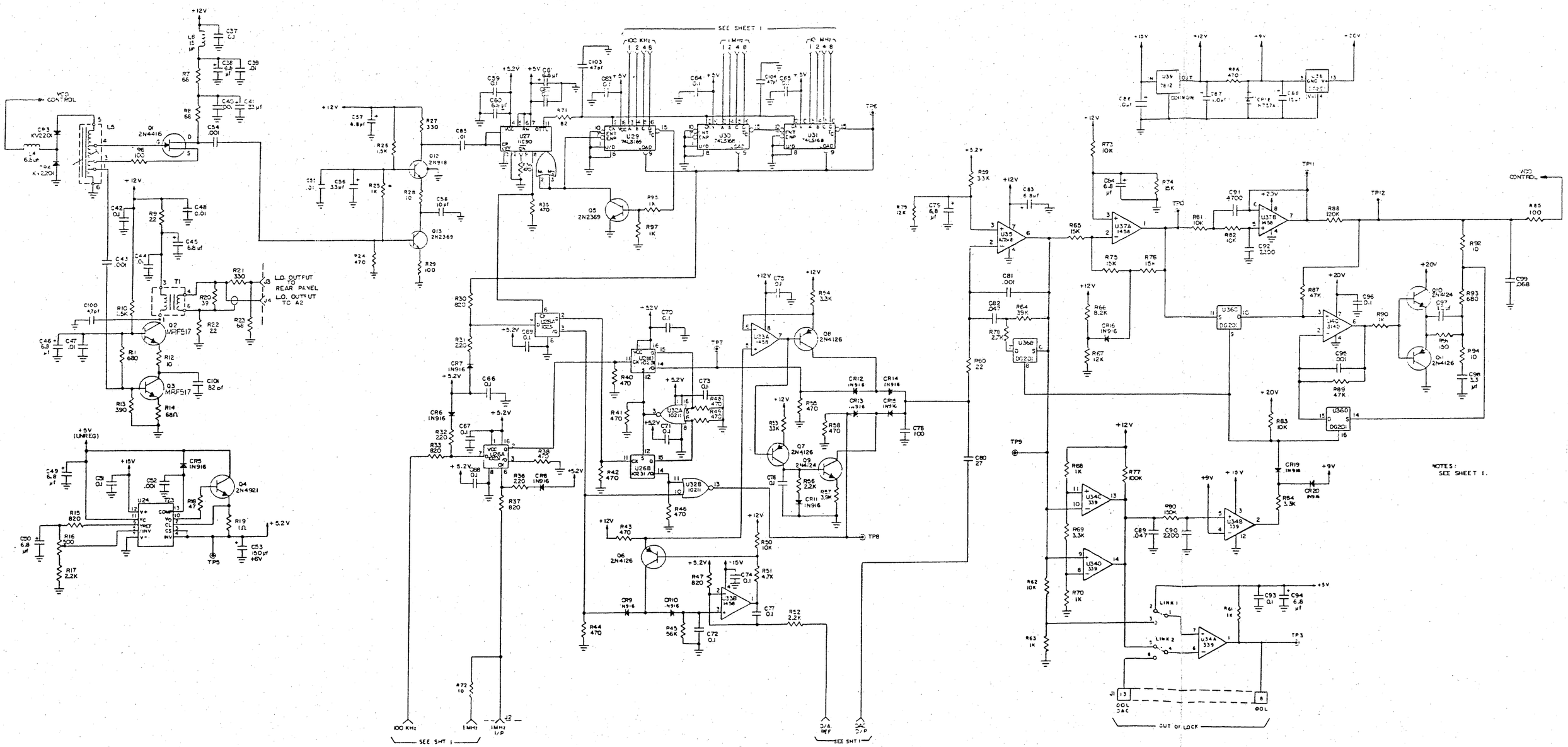


Figure 7-8. Schematic Diagram (09256), First LO Synthesizer (A7) (Sheet 2)

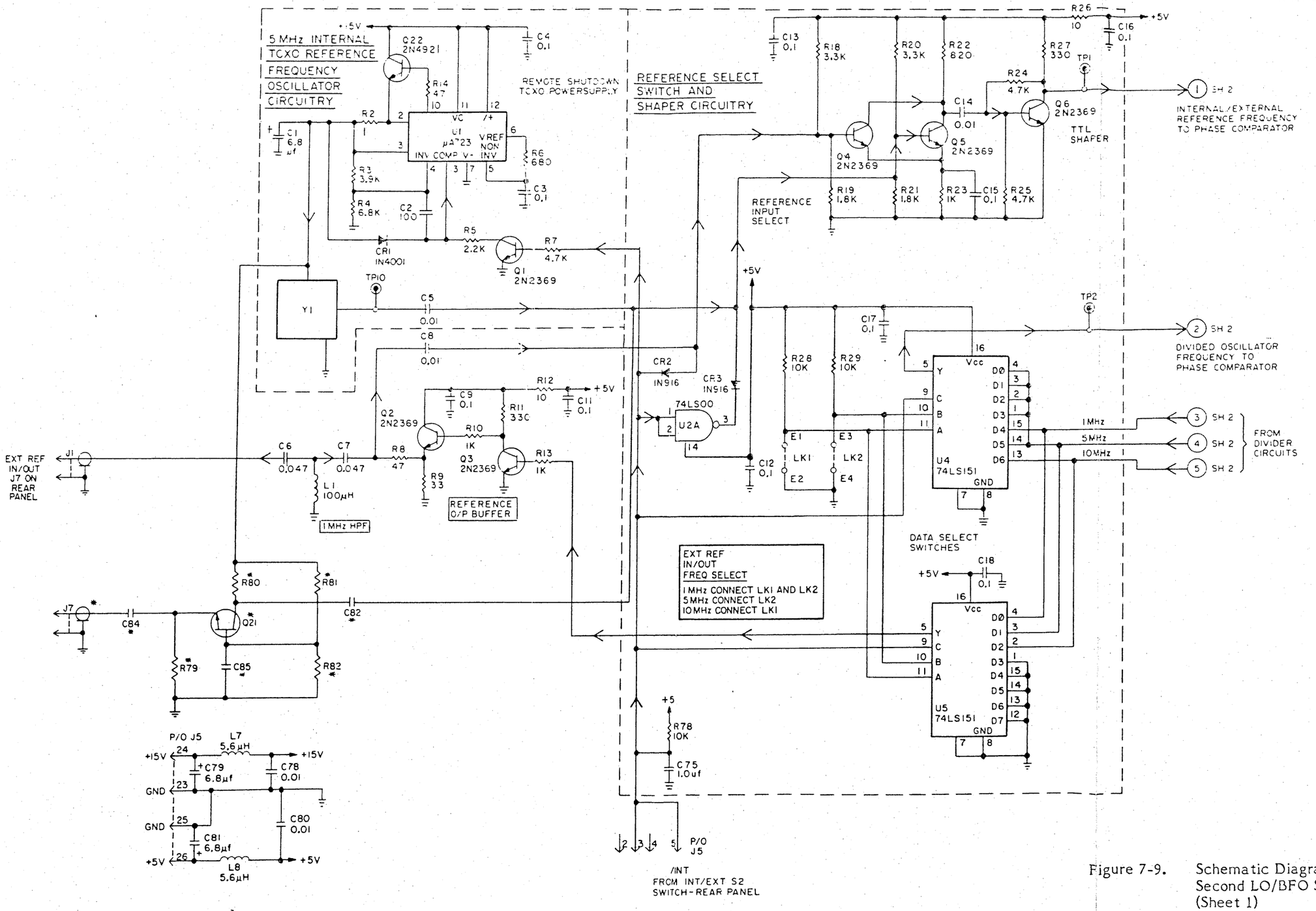


Figure 7-9. Schematic Diagram (09633), Second LO/BFO Synthesizer (A8) (Sheet 1)

PHASE COMPARATOR

20 MHz VCO CIRCUITRY

DIVIDE-BY-2000 CIRCUITRY (BFO CIRCUIT)

D/A CONVERTER CIRCUIT

OUT-OF-LOCK DETECTOR CIRCUIT

20 MHz XTAL OSCILLATOR

TTL SHAPER BUFFER/AMPLIFIER CIRCUITRY

DIVIDER CIRCUITRY

FREQUENCY DOUBLER CIRCUITRY

SH 1 (1) INT/EXT REFERENCE FROM TTL SHAPER CIRCUIT

SH 1 (2) DIVIDED OSC. FREQUENCY

SH 1 TO DATA SELECT CIRCUITS

1 MHz

5 MHz

10 MHz

U3A 74LS74

U3B 74LS74

U6 74LS90

U7B 74LS74

U7A 74LS74

U8 74LS390 DIVIDE BY 100

U9 74LS390 DIVIDE BY 20

U22A 10115

U22B 10115

U22C 10115

U22D 10115

U2B 74LS00

U2C 74LS00

U2D 74LS00

U11C 74LS00

U13D 74LS08

U11B 74LS00

Q7 2N3904

Q8 2N4126

Q9 2N3904

Q10 2N2369

Q11 2N2369

CR4 KV634 (MV1634)

Y2 20MHz

L2 1uH

L9

L10

J9 10 KHz OUT

6 SH 3 500 Hz TO PHASE COMPARATOR (BFO CIRCUITS)

J2 1 MHz TO A7

J3 40 MHz OUTPUT TO A3

J8 20 MHz OUTPUT TO A14

Figure 7-9. Schematic Diagram (09633), Second LO/BFO Synthesizer (A8) (Sheet 2)

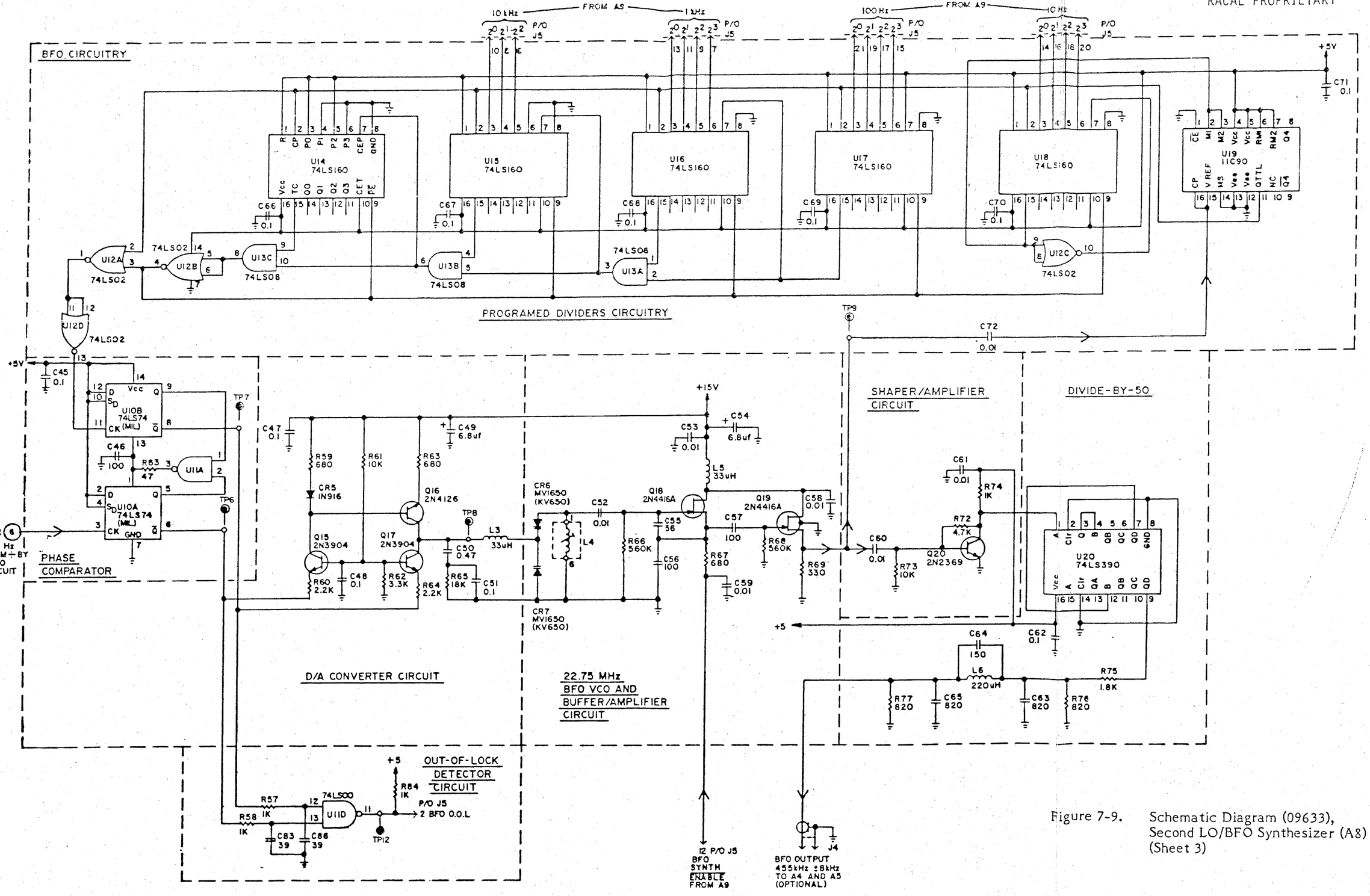


Figure 7-9. Schematic Diagram (09633), Second LO/BFO Synthesizer (A8) (Sheet 3)

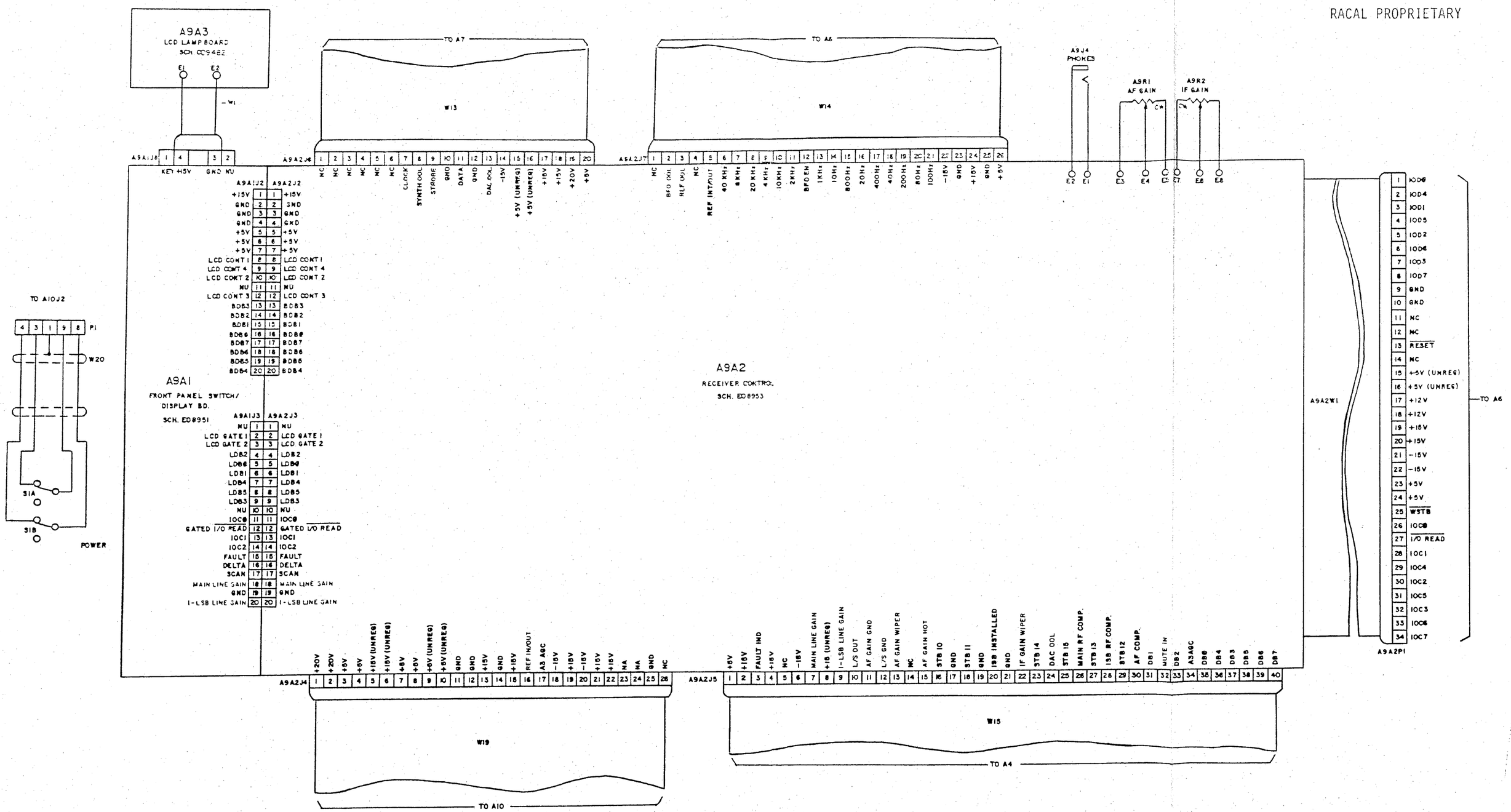


Figure 7-10 Interconnection Wiring Diagram (09024), Front Panel Assembly (A9)

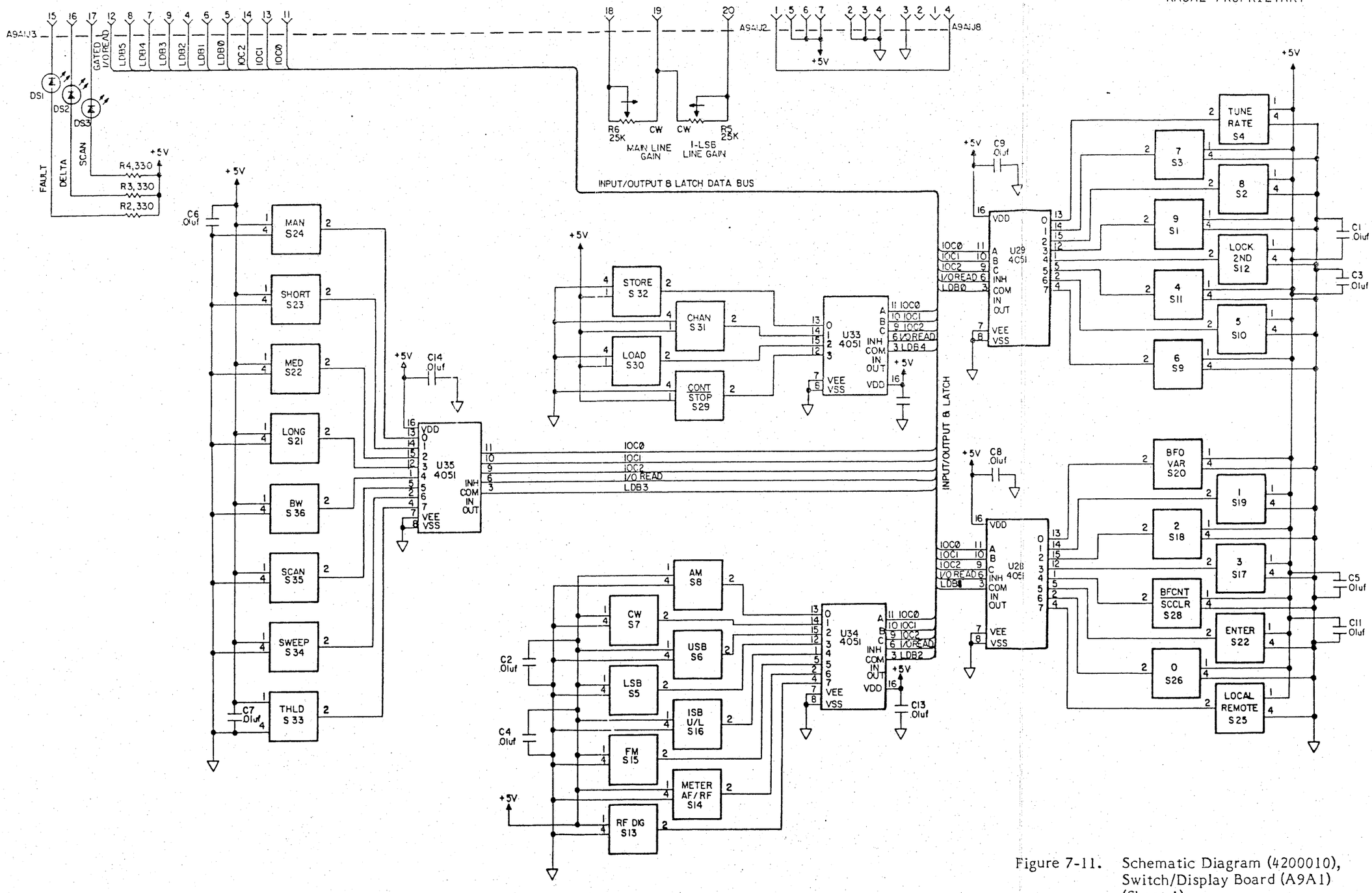


Figure 7-11. Schematic Diagram (4200010), Switch/Display Board (A9A1) (Sheet 1)

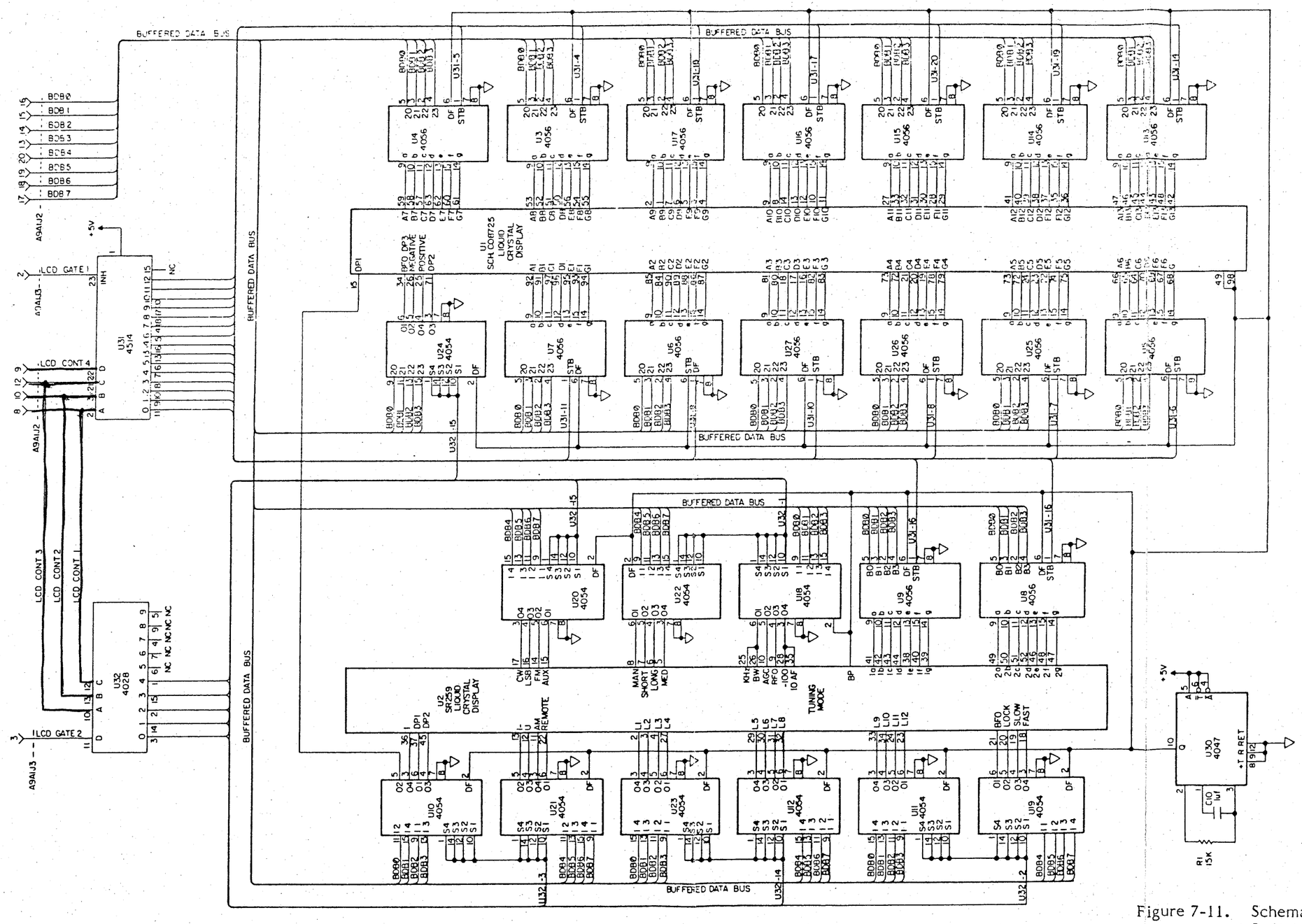


Figure 7-11. Schematic Diagram (4200010), Switch/Display Board (A9A1) (Sheet 2)

Figure 7-12. Schematic Diagram (08953) Receiver Control (A9A2)

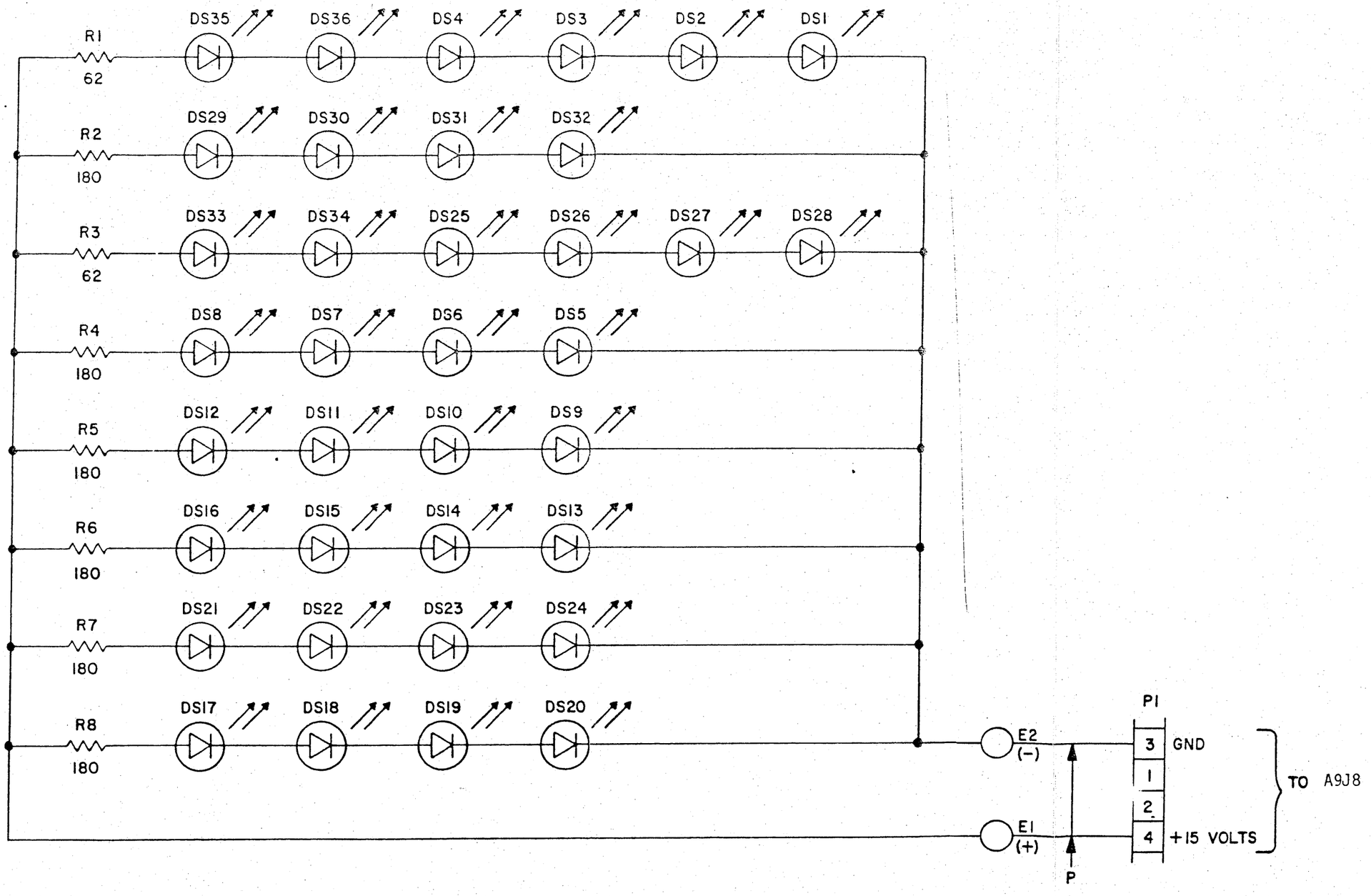


Figure 7-13. Schematic Diagram (09482), LCD/LED Display Board (A9A3)

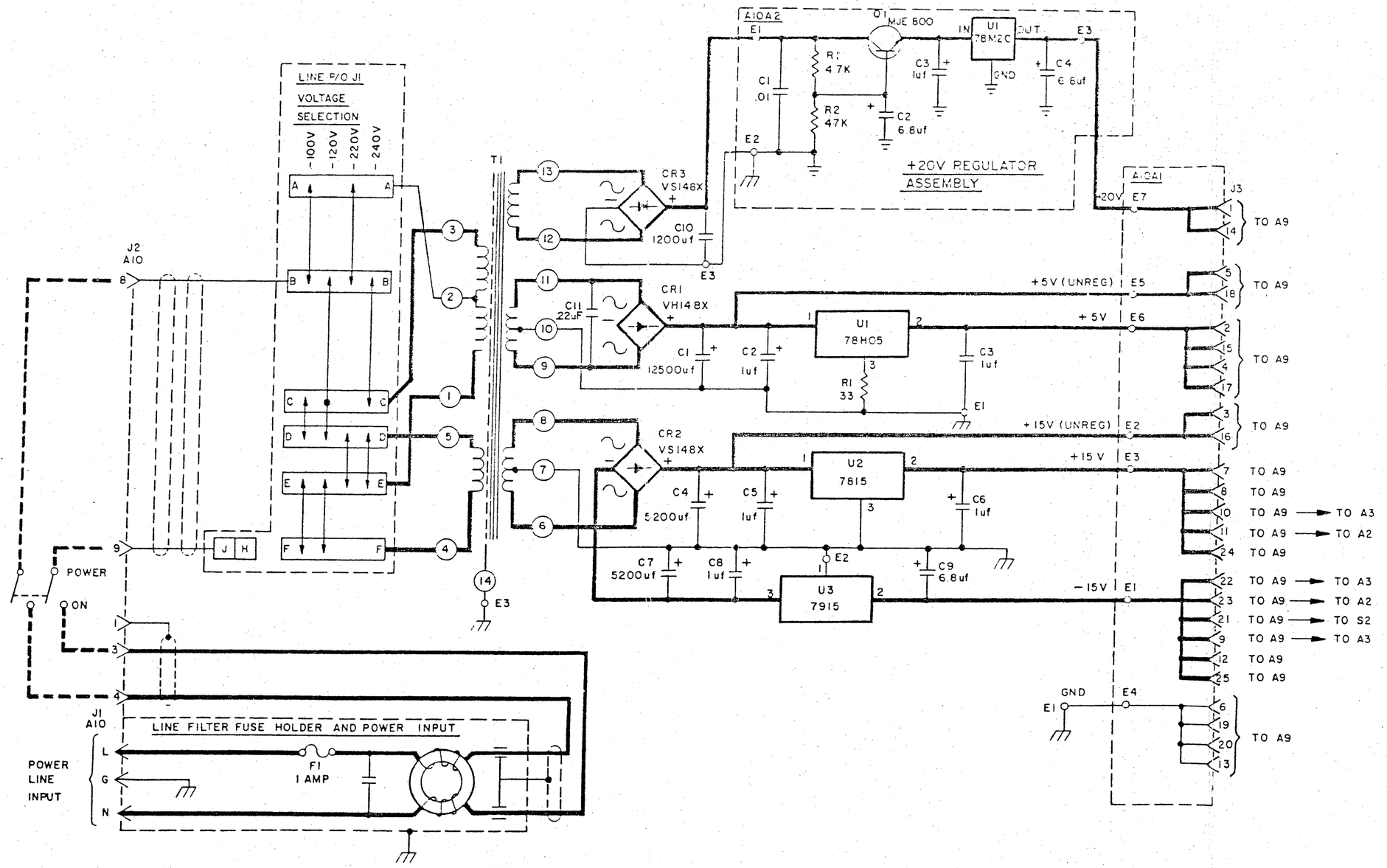


Figure 7-14. Schematic Diagram (8512) Power Supply (A10)

RF IN
A1W
A1
LOW PASS FILTER
A1W2
P
J5
P1
A2W1
E1
E2
RF IN
A2
1ST MIXER
J3
1st IF OUT
A2J2
GND
+15V
-15V
A2AGC
RIAS
A3W1
E1
E2
A3
2ND MIXER
E3
E4
A3W2
P1
J6
P
W1
P2
J1
2nd IF IN
A3J1
J2
A3J2
P2
REF INT/EXT
EXT
S2
INT
REAR PANEL
W2
W4
A4
MAIN IF/AF
WITHOUT ISB (A6)
WITH ISB (A6)
A4J7
J5
W16
NU
LINE AUDIO OUT
L/S OUT
L/S GND
NC
GND
MUTE CONTROL (NOTE 1)
GND
MAIN IF DIV. AGC
GND
NU
NU
FAULT MONITOR (NOTE 2)
NC
NC
NC
NC
NC
L1
L2
CT
ISB/USB AUDIO OUT
ISB/LSB AUDIO OUT
FRONT PANEL SELECTED AUDIO IN ISB
MAIN IF & ISB/USB DIV AGC
ISB/LSB DIV AGC
J4
P1
J2
MAIN IF OUT
MAIN IF OUT
BFO OUT
W10 (OPTIONAL)
W11 (OPTIONAL)
ISB/LSB IF OUT
A4J6
P1
J1
P2
J3
ISB AGC B
ISB AGC A
IDB 7
IF GAIN
IDB 6
ISB FITTED
GND
IDB 5
GND
IDB 4
NC
IDB 3
ISB DIV AGC
IDB 1
NC
IDB 2
+15V
IDB 0
NC
NC
LINE 2 OUT
OP3B
CT
OP3A
LINE 1 OUT
DAC
LINE 1 OUT
ISB AUDIO
LINE 2 OUT
LINE 1 IN
CT
LINE 2 IN
+15V
+15V
A5
OPTIONAL MODULE LOCATION
J2
ISB IF OUT
J9
(OPTIONAL)
P2
J4
1st LO OUT
A7
1ST LO SYNTHESIZER
A7J1
NC
NC
NC
NC
NC
CLOCK
SYNTH OOL
STROBE
GND
DATA
GND
NC
-15V
+5V UNREG
+5V UNREG
+5V
+15V
+15V
+20V
+5V
J2
P1
W3
P2
J2
P2
J3
2nd LO OUT
A8
2ND LO/BFO SYNTHESIZER
A8J5
NC
OOL BFO
OOL REF
NC
REF INT/EXT
40 KHz
8 KHz
20 KHz
4 KHz
10KHz
2KHz
BFO EN
1 KHz
10 Hz
800 Hz
20 Hz
40 Hz
200 Hz
80 Hz
10Hz
+15V
GND
+5V
REF IN/OUT
J1
P1
W7
J4
P1
W6
P2
J5
BFO OUT
BFO IN
A6J12
+5V
+15V
FAULT IND
+15V
NC
-15V
MAIN AF LEVEL
+15V UNREG
ISB AF LEVEL
PHONE OUT
VOL GND
PHONE GND
VOL O/P
NC
VOL I/P
STB 10
GND
STB 11
GND
ISB FITTED
GND
ISB GAIN
STB 14
DAC
STB 15
MAIN RF COMP
STB 13
ISB RF COMP
STB 12
AF COMP
DB 1
NC
DB 2
A3 AGC
IDB4
DB 3
DB 5
DB 6
+15V
+15V
P1
W13
W14
W15
P2
J7
REF IN/OUT
REAR PANEL
A10J3
P3
P1
+20V
+5V
+15V UNREG
+5V
+5V UNREG
GND
+15V
+15V
A3 AGC
+15V
MUTE OUT
GND
+20V
-5V
+15V UNREG
+5V
+5V UNREG
GND
GND
REF INT/EXT
-15V
-15V
+15V
MUTE CONTROL
A10
POWER SUPPLY
W18
A10J1
POWER CORD
REAR PANEL
W19
NC
A10J2
W20
S1
POWER
A9
FRONT PANEL ASSEMBLY
A9W1
A6A2
MICROCOMPUTER
A6A1
OPTIONAL INTERFACE

Figure 7-15. Interconnection Wiring Diagram (5200002), Main Chassis Assembly